

LCFC Confidential


ACLUA M/B Schematics Document

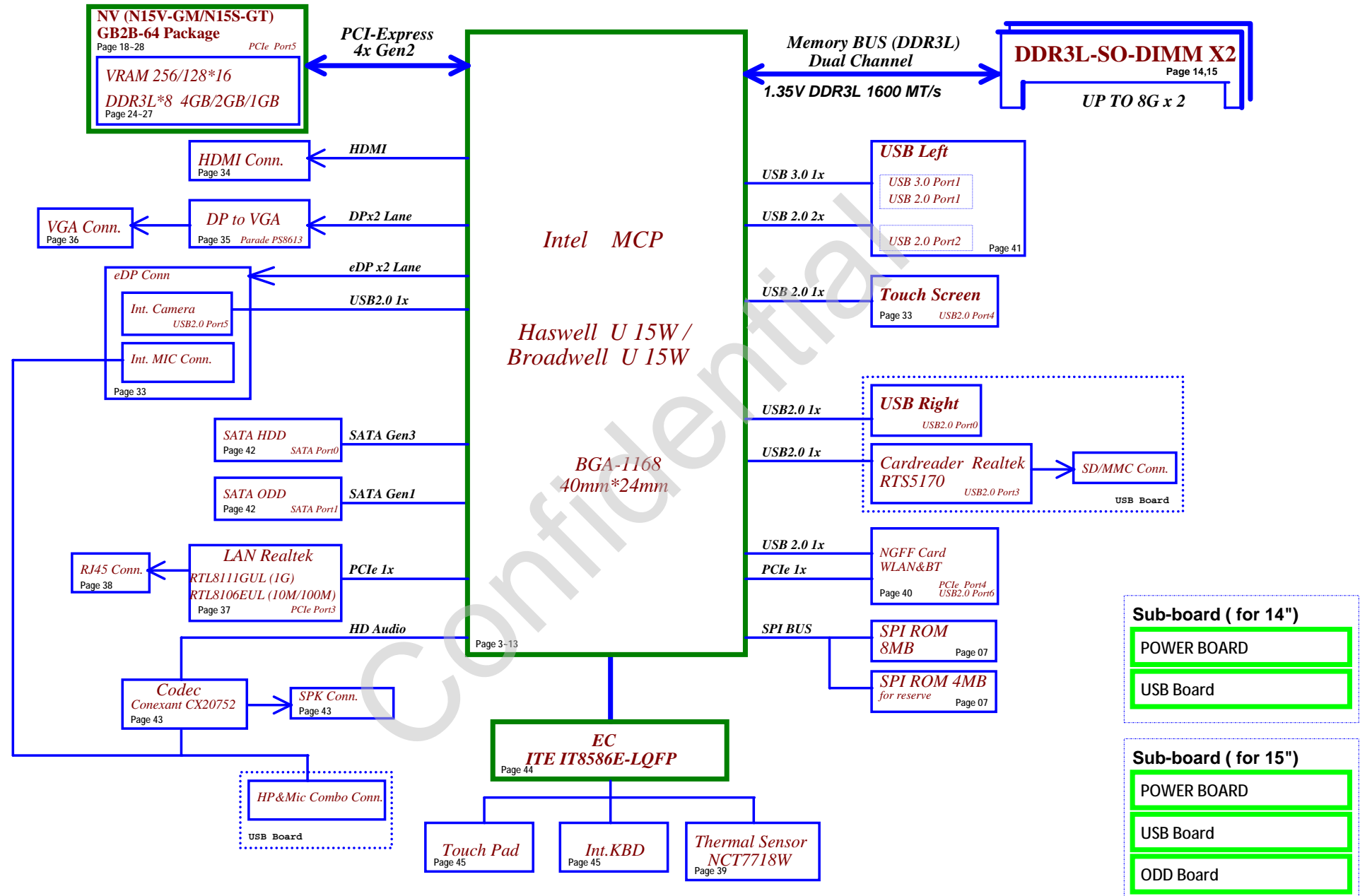
Intel Haswell/Broadwell U-Processor with DDRIII L + NV (N15V-GM/N15S-GT) GPU


2013-12-26

REV: 0.3

Confidential

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Security Classification	LC Future Center Secret Data		Title	 Block Diagram
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
100M@	100M LAN Part
GIGA@	GIGA LAN Part
OPT@	Discrete GPU SKU part
N15SGT@	For N15S-GT GPU part
N15VGM@	For N15V-GM part
GC6@	GC62.0 support part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
UMA@	UMA SKU part
TS@	For support touch panel sku part
AOAC@	AOAC support part
ME@	ME part(connector, hole)

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCI PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001_100xb
VGA	0x41(default)
PCH	need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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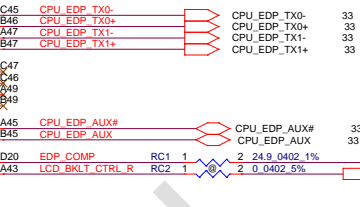
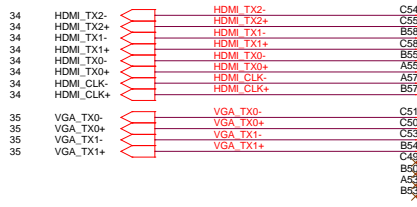
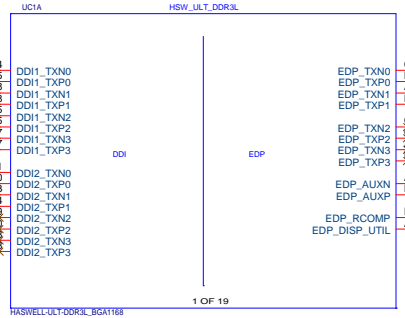
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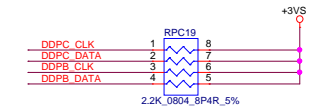
ACLJA

HDMI D2
HDMI D1
HDMI D0
HDMI CLK
DP TO VGA Converter

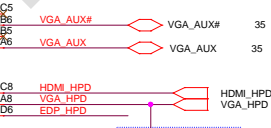
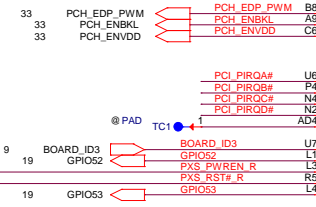
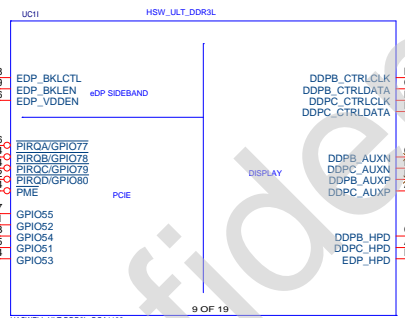
DP TO VGA Converter



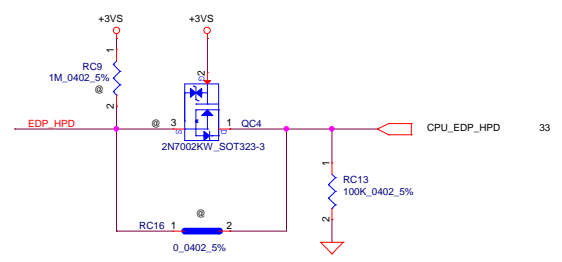
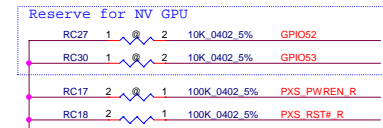
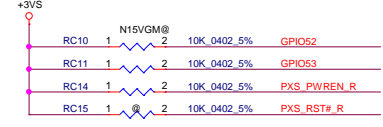
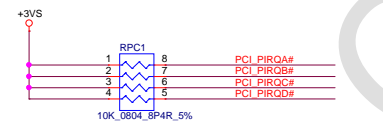
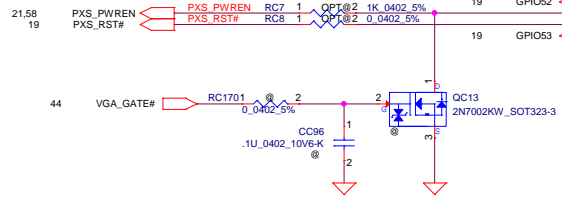
+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil



DDPC_CTRLDATA
The signal has a weak internal pull-down.
* H Port is not detected.
L Port is not detected.

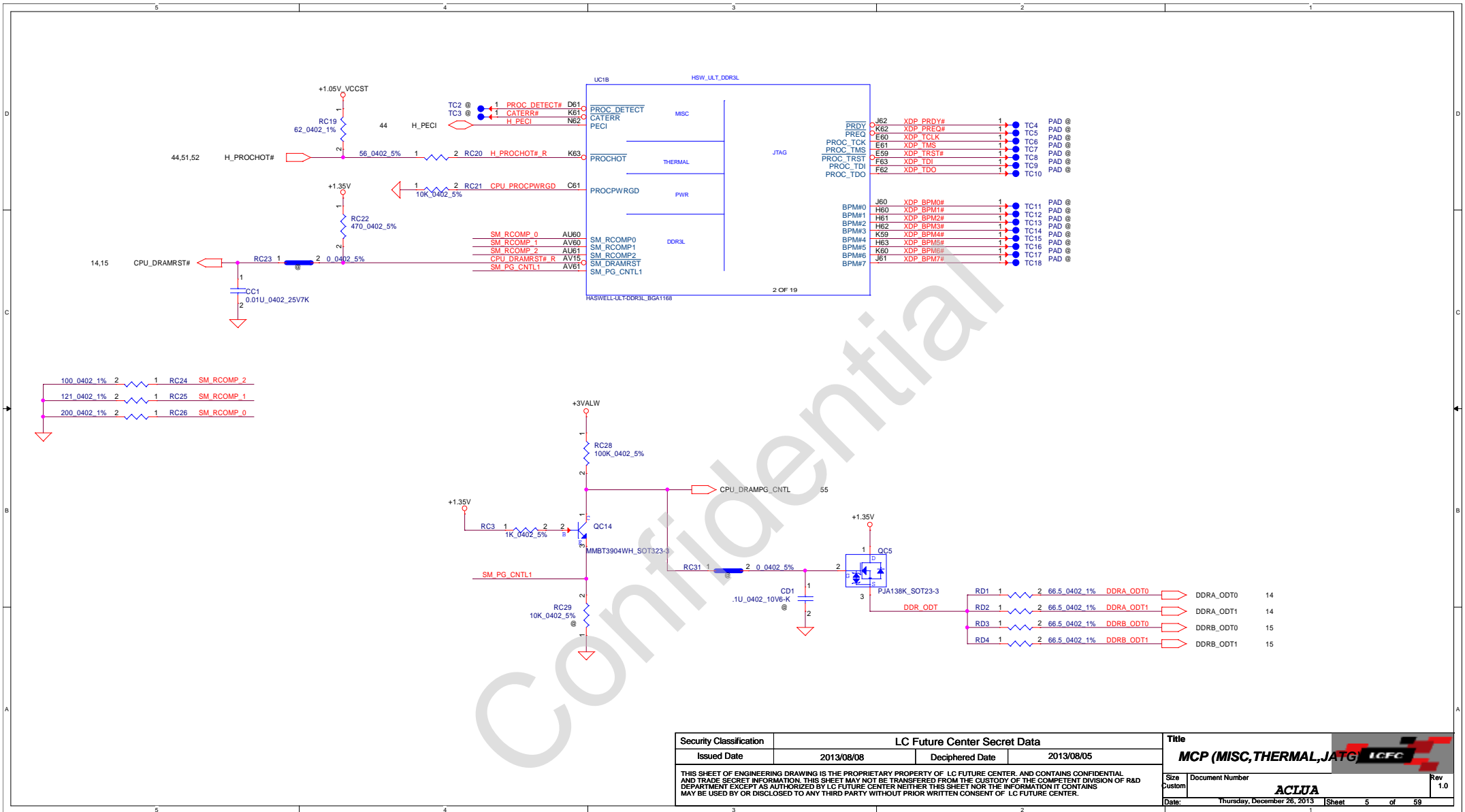


After confirm with vendor, HPD has internal pull-down ~100K at PS8613, just reserve in case. RC37 can be removed next phase if no issue.



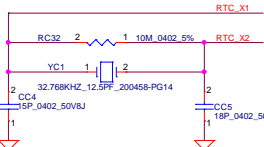
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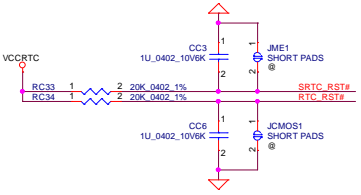


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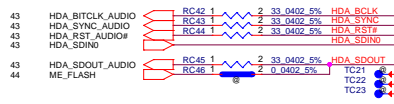
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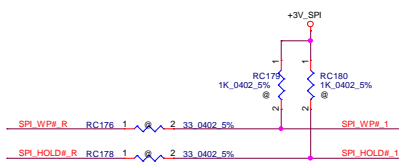
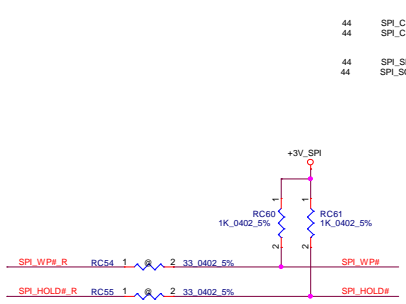
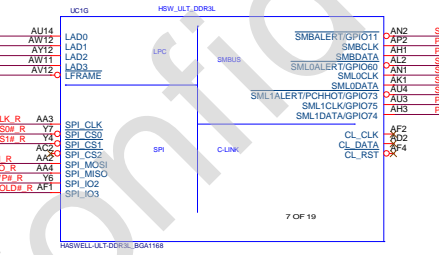
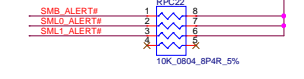
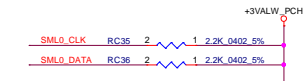
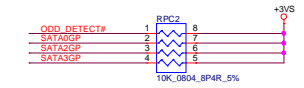
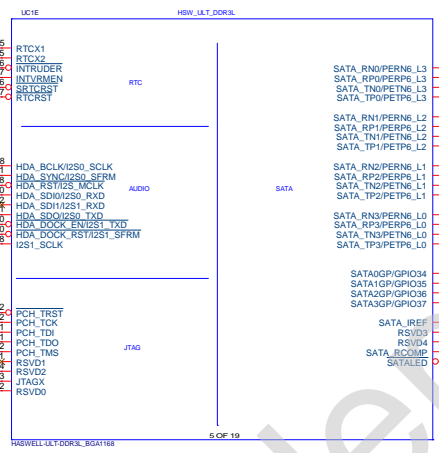
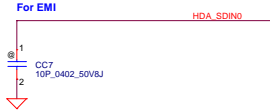
CRYSTAL
 1. Space 15MIL
 2. No trace under crystal
 3. Place on opposite side of MCP for temp influence



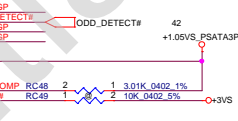
INTVRMEN
 * H Integrated VRM enable (Default)
 L Integrated VRM disable
 (INTVRMEN should always be pull high.)



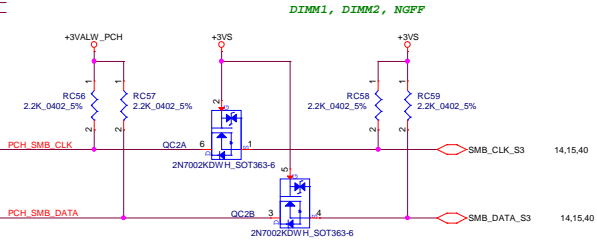
* HDA_SDO This signal has a weak internal pull-down.
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



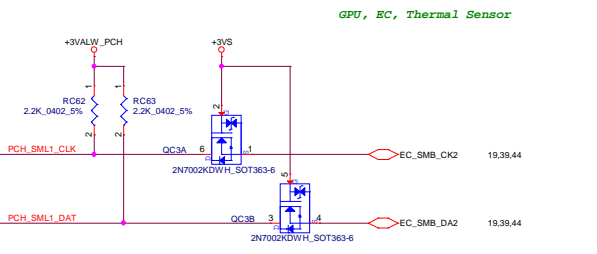
+3V SPI
 1. If support DS3, connect to +3VS and don't support EC mirror code;
 * 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



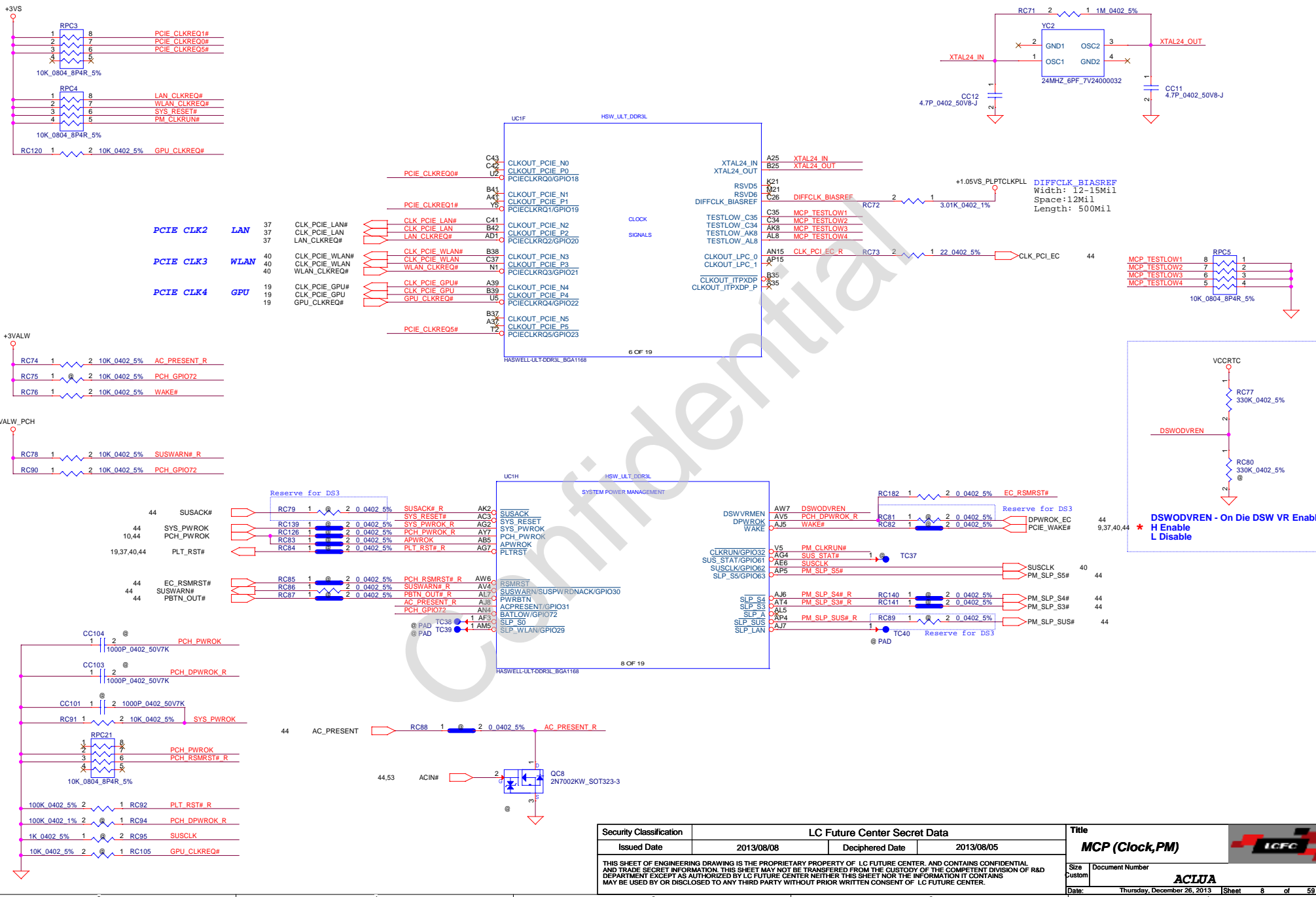
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 Space: 12mil
 Length: 500mil



DIMM1, DIMM2, NGFF

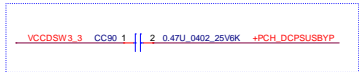
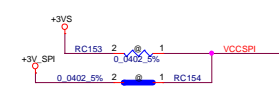
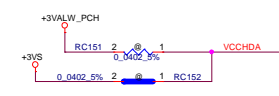
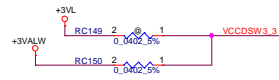
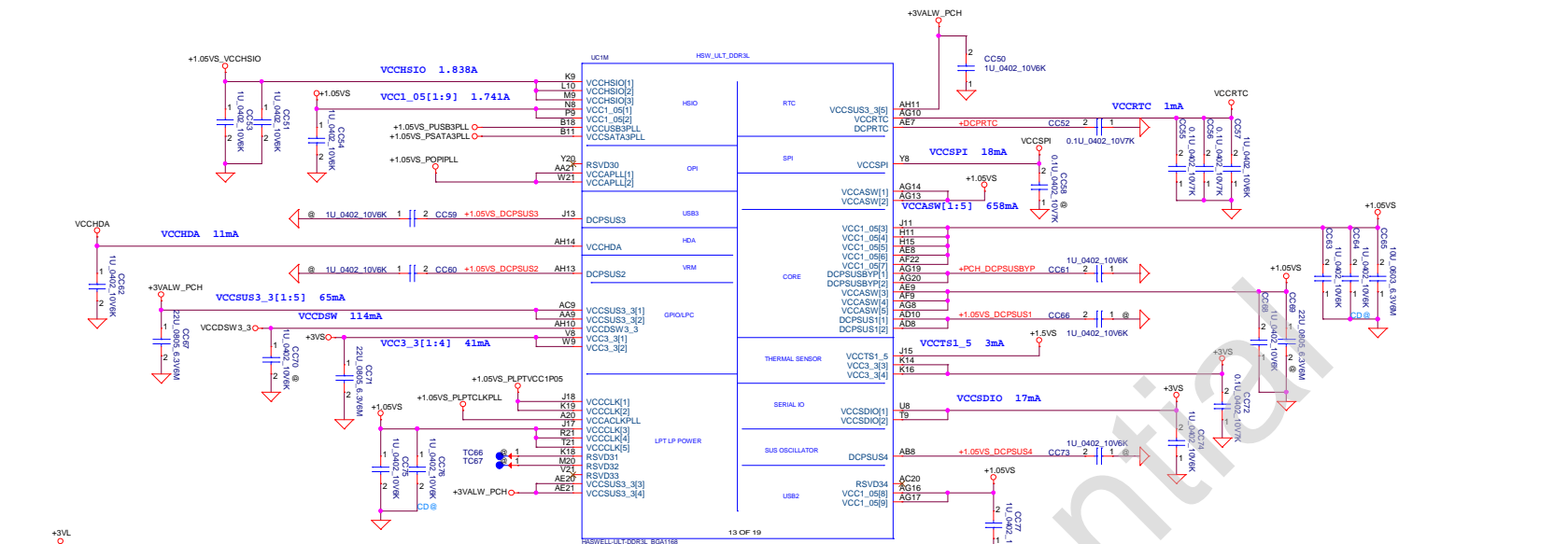


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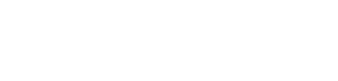
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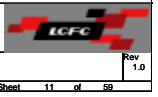


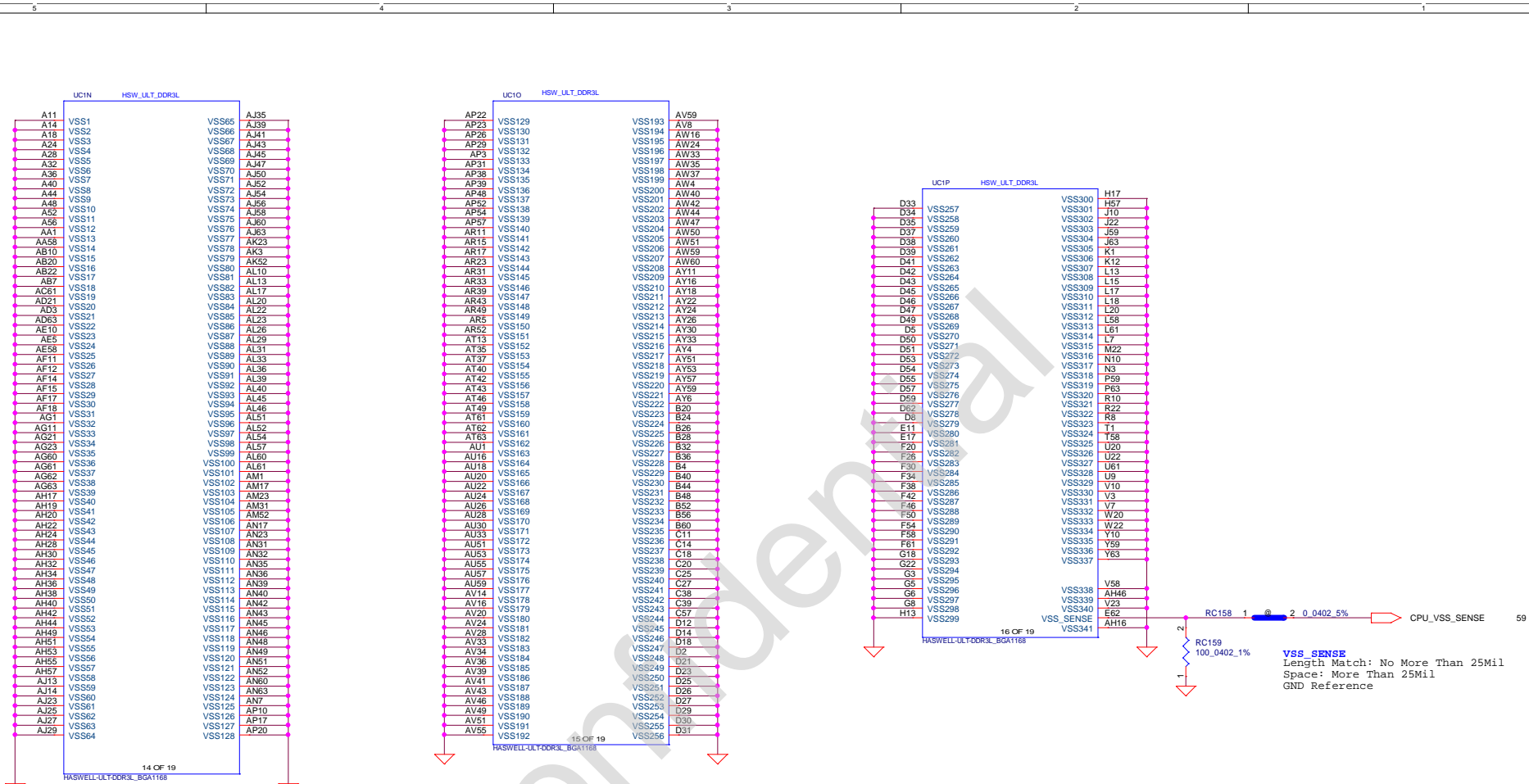
For Intel recommend, place one 0.47uF capacitor to address temporary inrush current. (DOC. 48999)

Need short




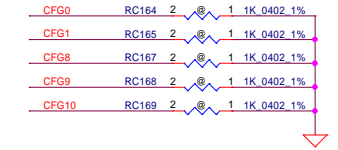
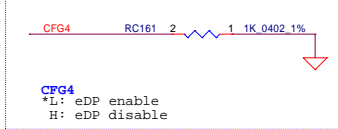
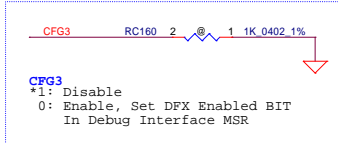
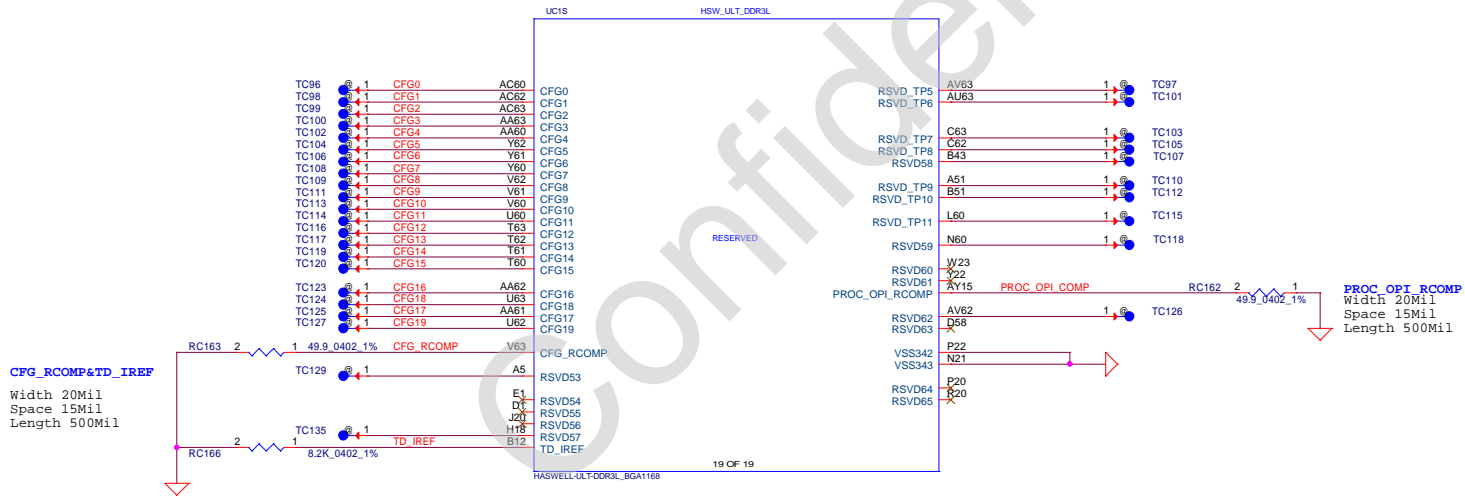
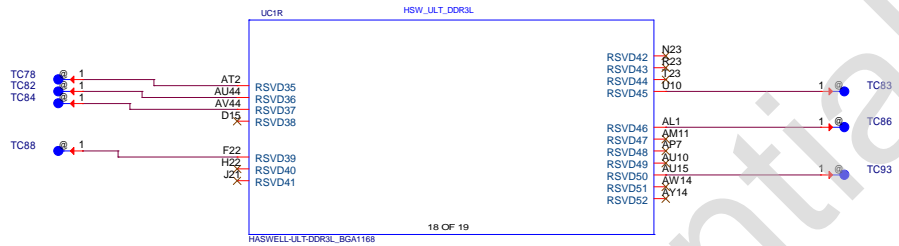
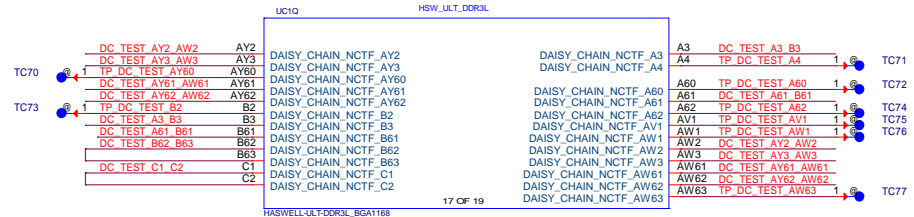
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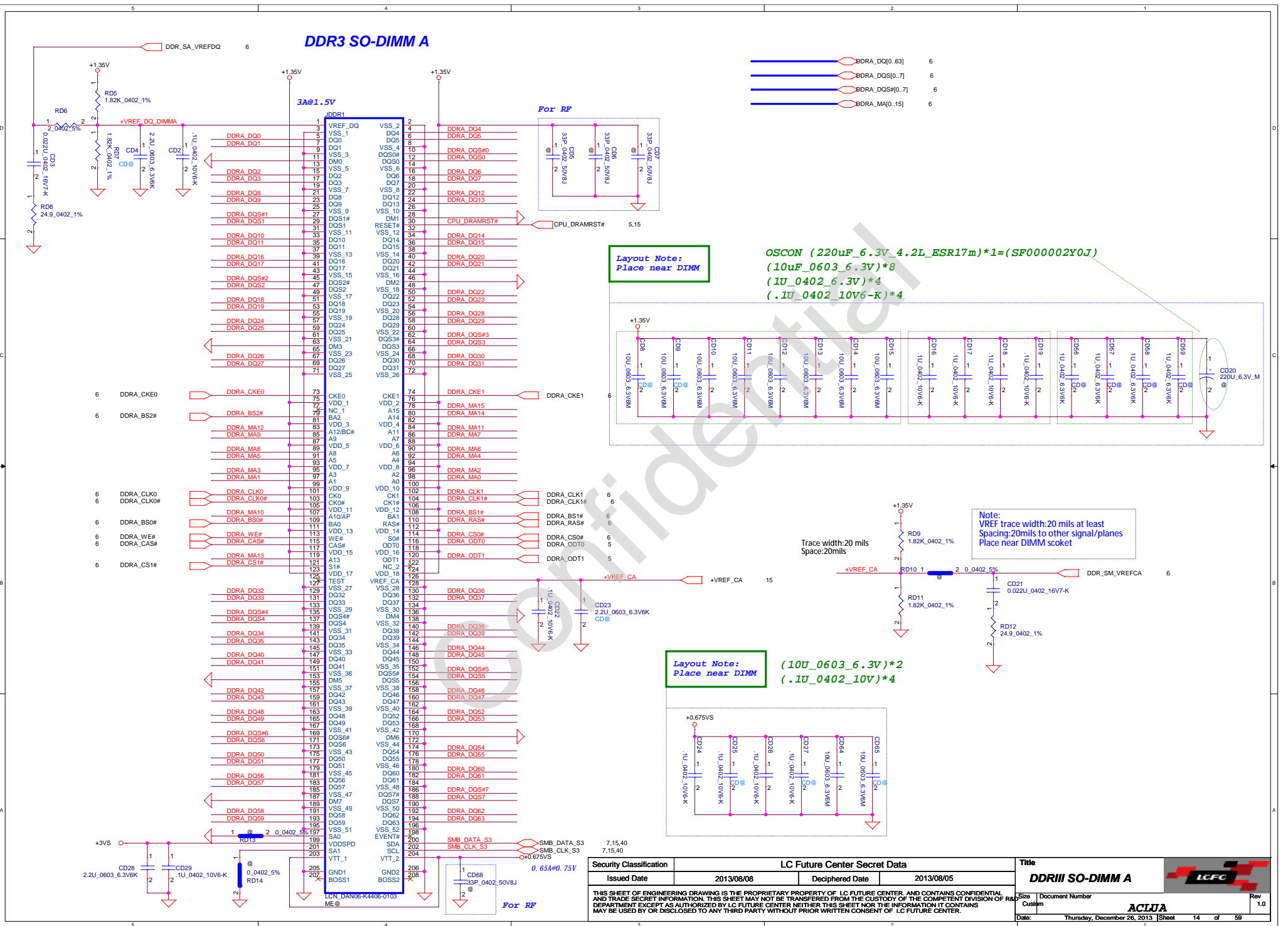
VSS_SENSE
 Length Match: No More Than 25Mil
 Space: More Than 25Mil
 GND Reference

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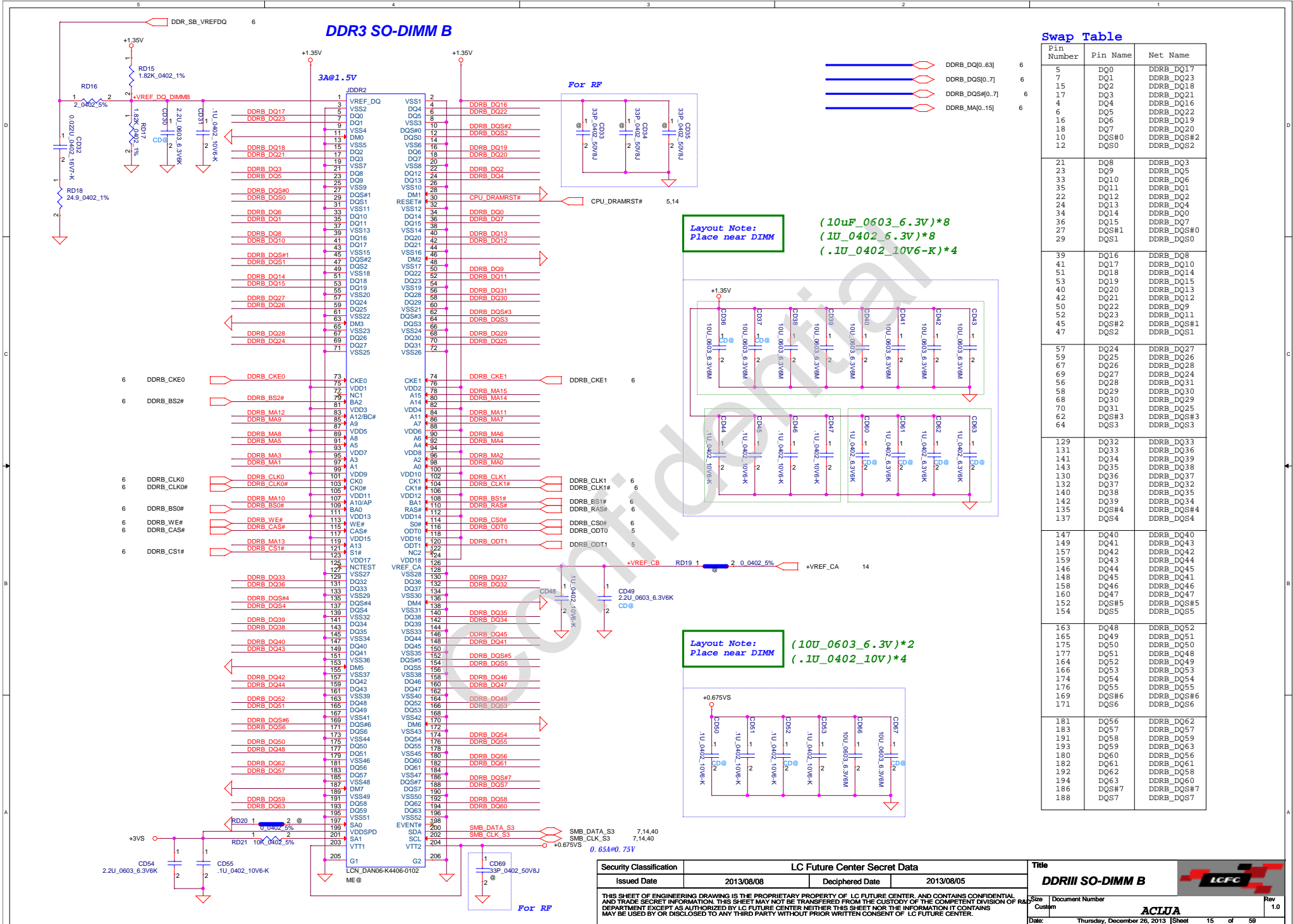


CFG_RCOMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil

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DDR3 SO-DIMM B



Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR3_DQ0
7	DQ1	DDR3_DQ1
15	DQ2	DDR3_DQ2
17	DQ3	DDR3_DQ3
4	DQ4	DDR3_DQ4
6	DQ5	DDR3_DQ5
9	DQ6	DDR3_DQ6
16	DQ7	DDR3_DQ7
18	DQ8	DDR3_DQ8
10	DQ9	DDR3_DQ9
12	DQ10	DDR3_DQ10
21	DQ11	DDR3_DQ11
23	DQ12	DDR3_DQ12
33	DQ13	DDR3_DQ13
35	DQ14	DDR3_DQ14
22	DQ15	DDR3_DQ15
24	DQ16	DDR3_DQ16
34	DQ17	DDR3_DQ17
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142	DQ47	DDR3_DQ47
135	DQ48	DDR3_DQ48
137	DQ49	DDR3_DQ49
147	DQ50	DDR3_DQ50
149	DQ51	DDR3_DQ51
157	DQ52	DDR3_DQ52
159	DQ53	DDR3_DQ53
146	DQ54	DDR3_DQ54
148	DQ55	DDR3_DQ55
158	DQ56	DDR3_DQ56
160	DQ57	DDR3_DQ57
152	DQ58	DDR3_DQ58
154	DQ59	DDR3_DQ59
163	DQ60	DDR3_DQ60
165	DQ61	DDR3_DQ61
175	DQ62	DDR3_DQ62
177	DQ63	DDR3_DQ63
164	DQ64	DDR3_DQ64
166	DQ65	DDR3_DQ65
174	DQ66	DDR3_DQ66
176	DQ67	DDR3_DQ67
169	DQ68	DDR3_DQ68
171	DQ69	DDR3_DQ69
181	DQ70	DDR3_DQ70
183	DQ71	DDR3_DQ71
191	DQ72	DDR3_DQ72
193	DQ73	DDR3_DQ73
180	DQ74	DDR3_DQ74
182	DQ75	DDR3_DQ75
192	DQ76	DDR3_DQ76
194	DQ77	DDR3_DQ77
186	DQ78	DDR3_DQ78
188	DQ79	DDR3_DQ79

Layout Note: Place near DIMM


(10uF_0603_6.3V)*8
(1U_0402_6.3V)*8
(.1U_0402_10V6-K)*4

Layout Note: Place near DIMM


(10U_0603_6.3V)*2
(.1U_0402_10V)*4

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

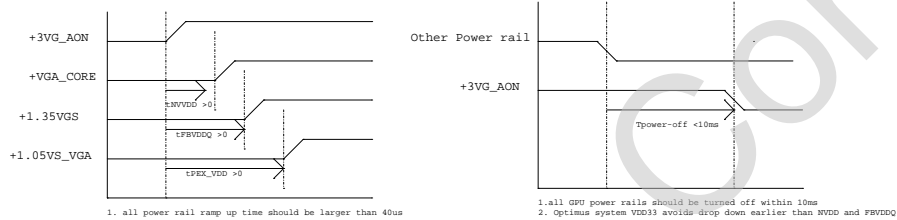
Products	GPU	Mem	NVCLK	NVVDD			FBVDD		FBVDDQ		PCI Express		I/O and PLLVDD		Other	
	(4)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 1GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

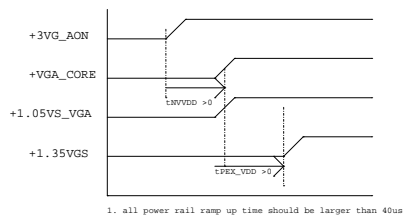
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



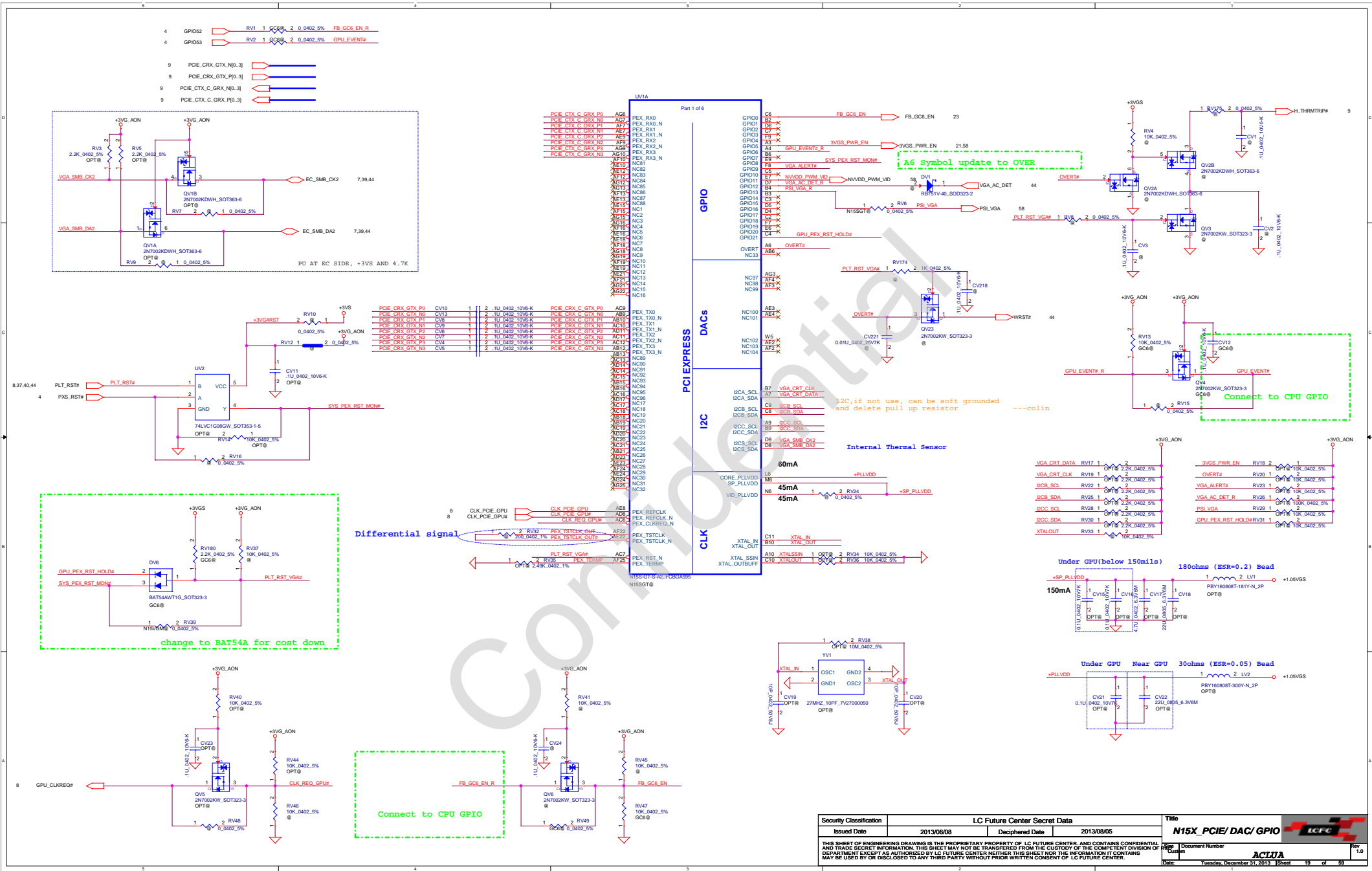
N15S-GT Power Sequence



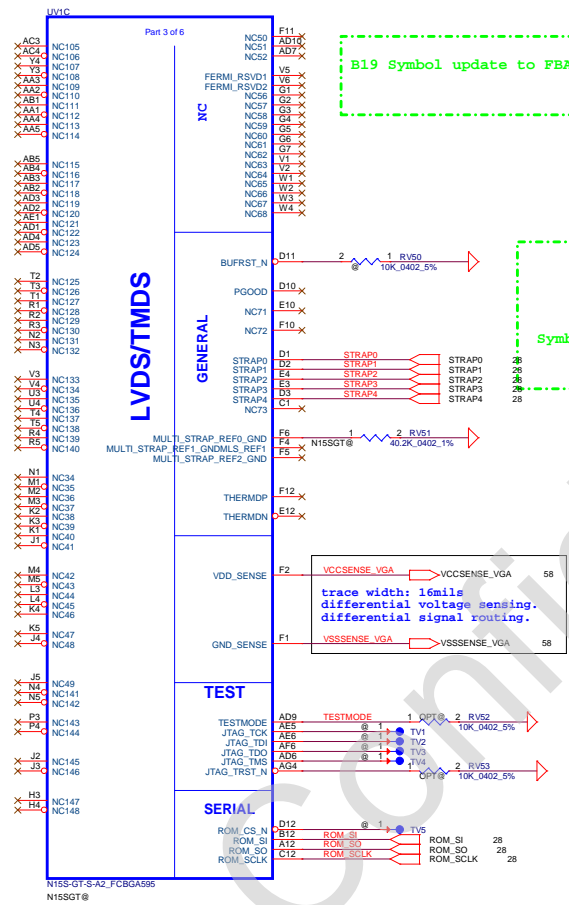
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

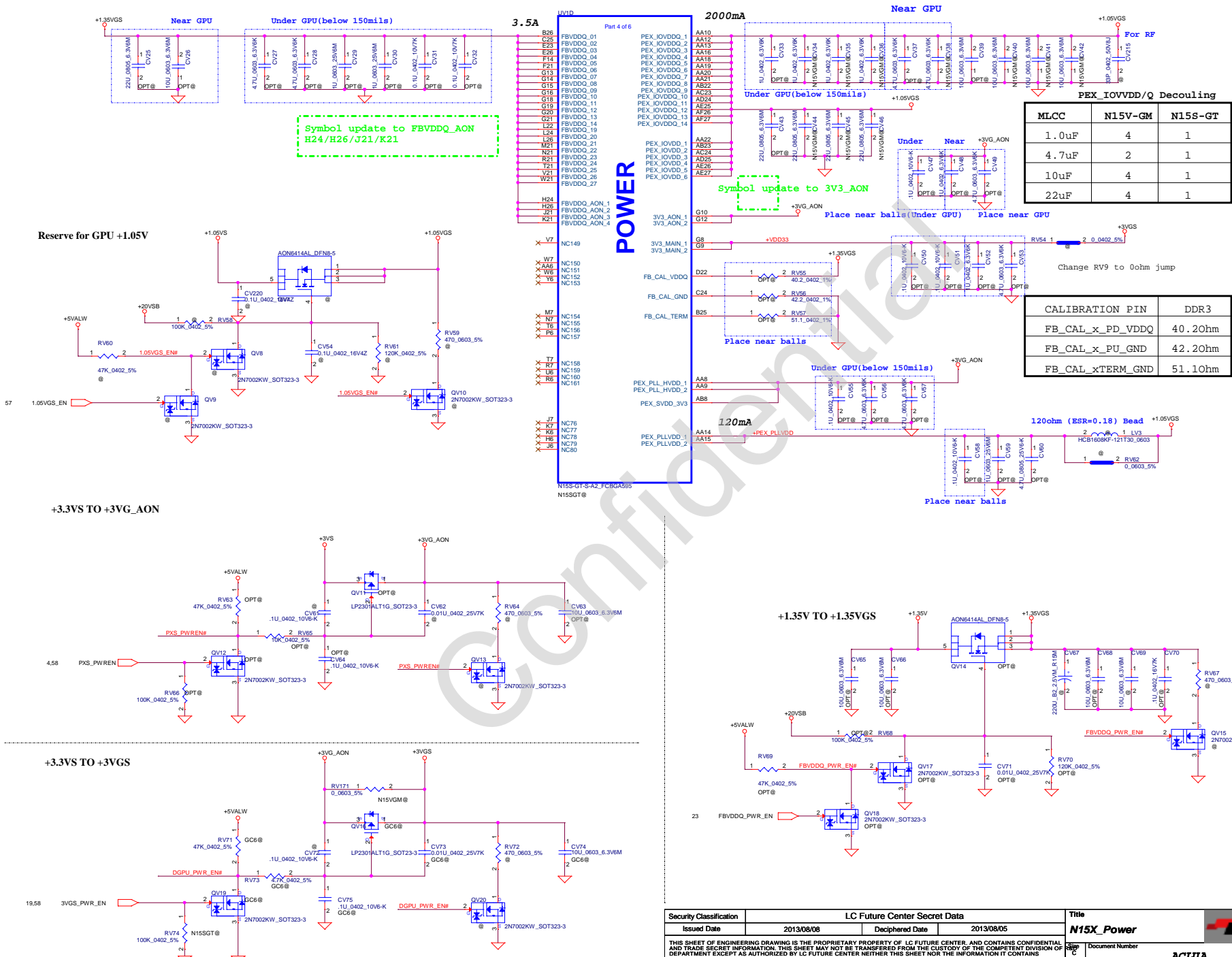
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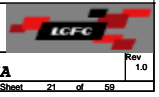


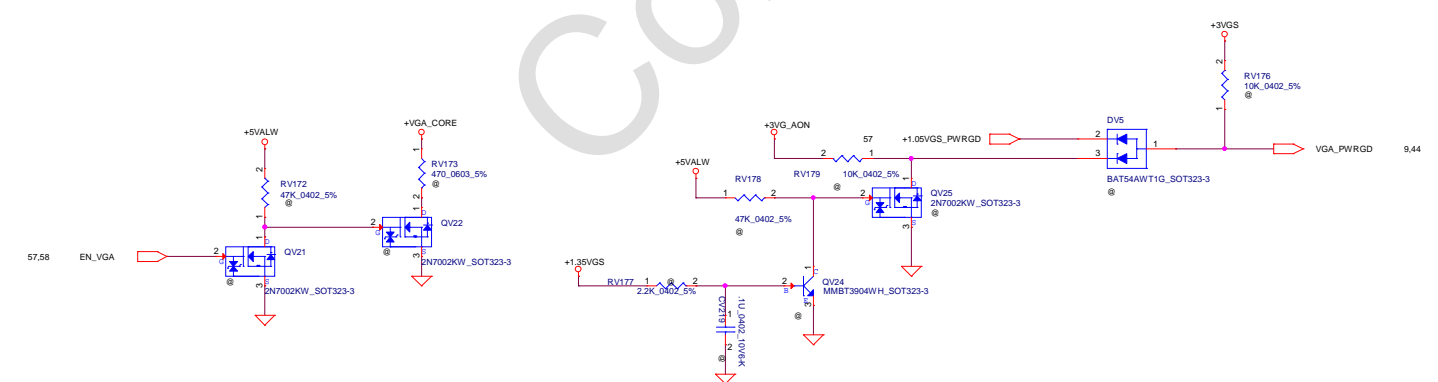
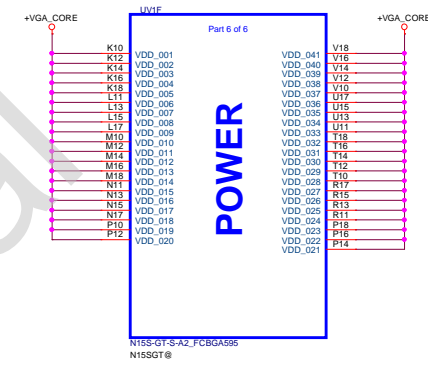
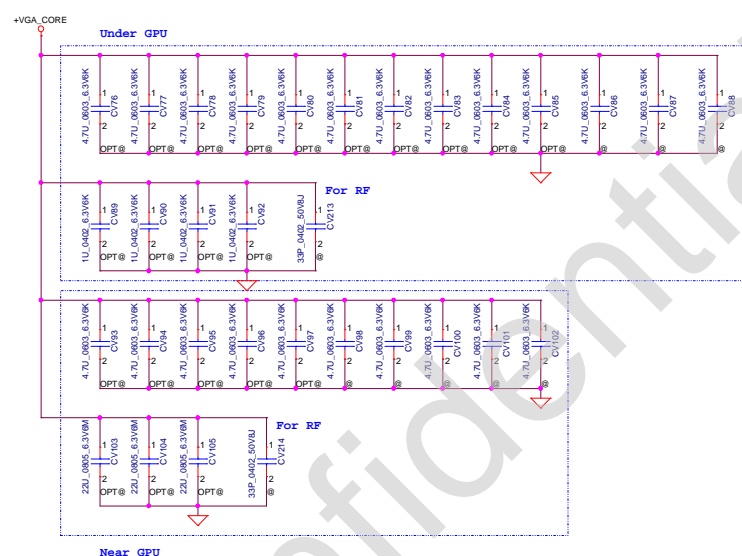
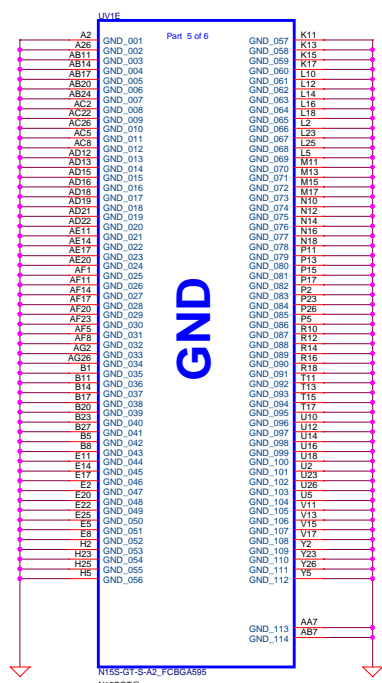
PEX_I/OVDD/Q Decoupling

MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1

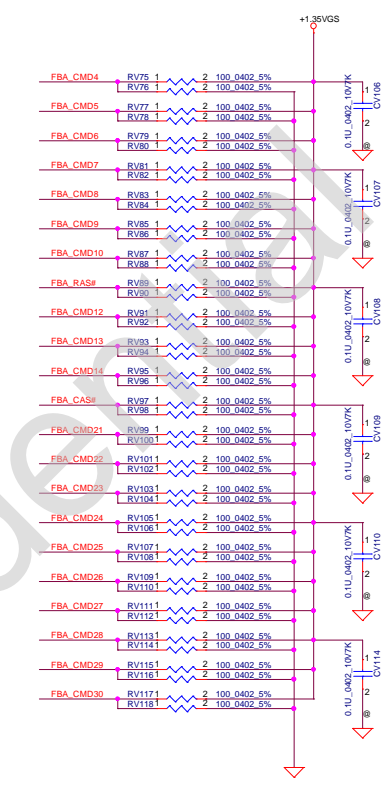
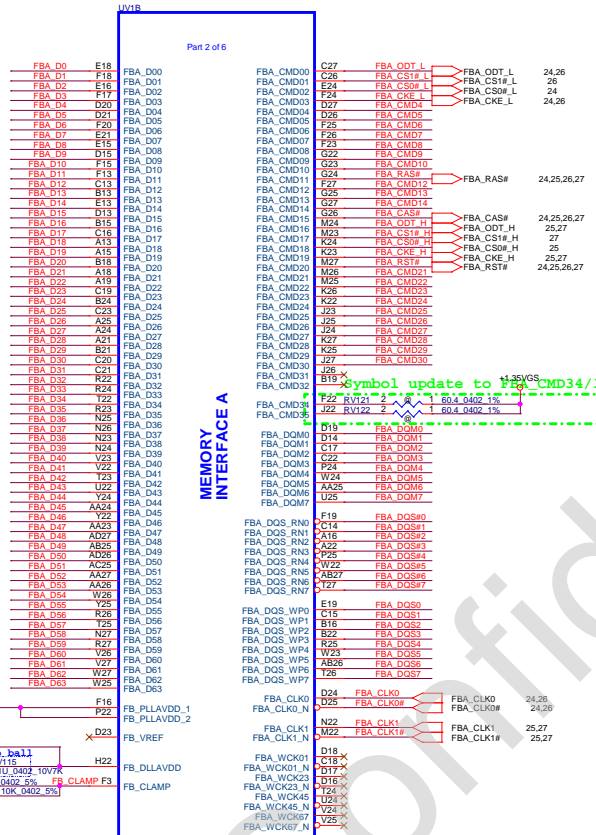
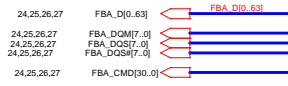
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_x_TERM_GND	51.1Ohm

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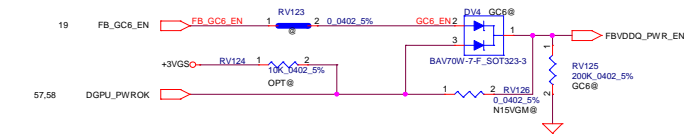
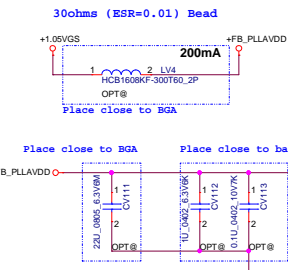


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CMD mapping mod Mode E

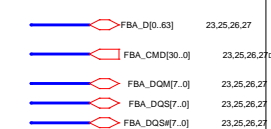
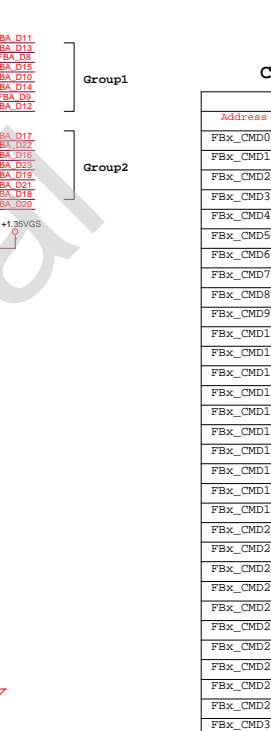
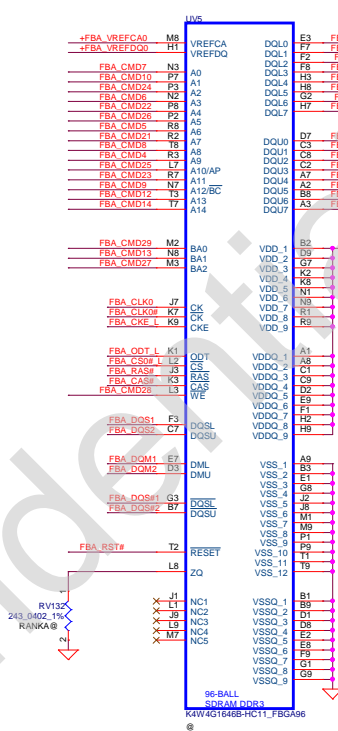
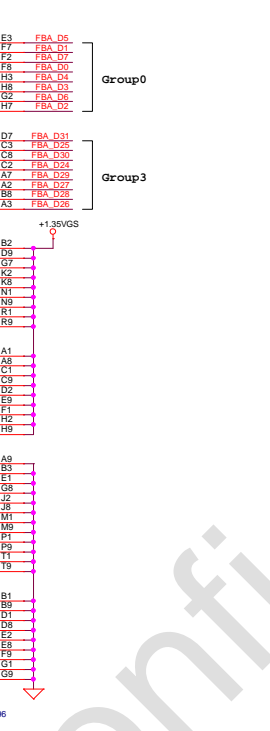
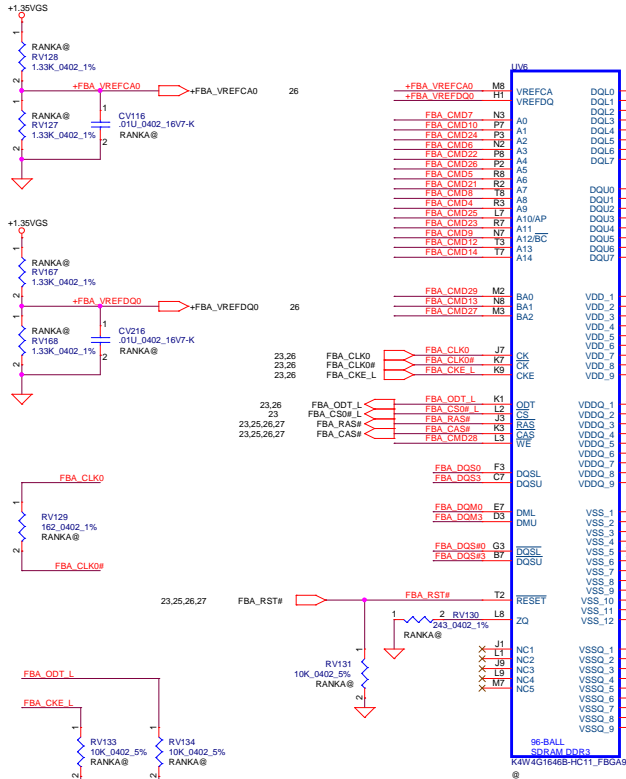
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FbxCMD0	ODT_L		ODT_L	
FbxCMD1			CSI#_L	
FbxCMD2	CS0#_L			
FbxCMD3	CKE_L		CKE_L	
FbxCMD4	A9	A9	A11	A11
FbxCMD5	A6	A6	A7	A7
FbxCMD6	A3	A3	BA1	BA1
FbxCMD7	A0	A0	A12	A12
FbxCMD8	A8	A8	A8	A8
FbxCMD9	A12	A12	A0	A0
FbxCMD10	A1	A1	A2	A2
FbxCMD11	RAS#	RAS#	RAS#	RAS#
FbxCMD12	A13	A13	A14	A14
FbxCMD13	BA1	BA1	A3	A3
FbxCMD14	A14	A14	A13	A13
FbxCMD15	CAS#	CAS#	CAS#	CAS#
FbxCMD16			ODT_H	ODT_H
FbxCMD17			CSI#_H	CSI#_H
FbxCMD18			CS0#_H	
FbxCMD19			CKE_H	CKE_H
FbxCMD20	RST	RST	RST	RST
FbxCMD21	A7	A7	A6	A6
FbxCMD22	A4	A4	A5	A5
FbxCMD23	A11	A11	A9	A9
FbxCMD24	A2	A2	A1	A1
FbxCMD25	A10	A10	WE#	WE#
FbxCMD26	A5	A5	A4	A4
FbxCMD27	BA2	BA2		
FbxCMD28	WE#	WE#	A10	A10
FbxCMD29	BA0	BA0	BA0	BA0
FbxCMD30			BA2	BA2



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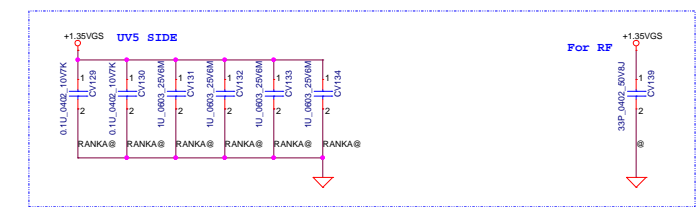
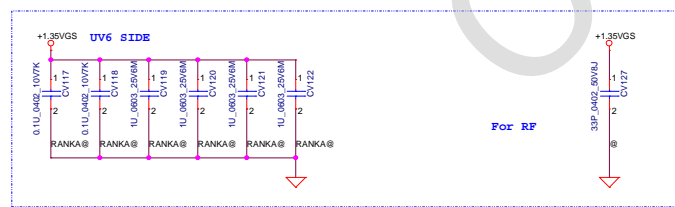
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at least 16 mils width(optimal)
20 mils spacing to other signals /planes



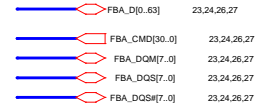
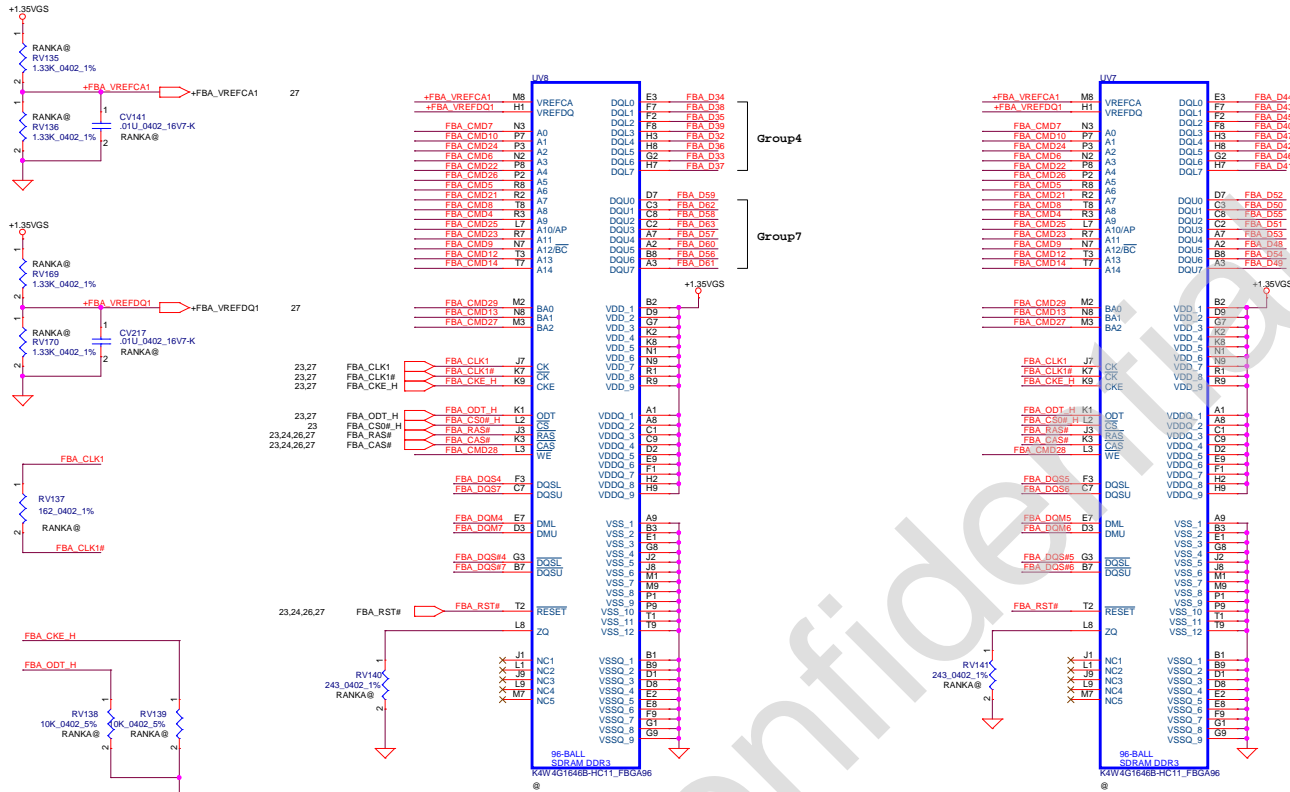
CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CS1#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	A13	A13	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16		ODT_H		ODT_H
FBX_CMD17			CS1#_H	
FBX_CMD18		CS0#_H		
FBX_CMD19		CKE_H		CKE_H
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30		BA2		BA2



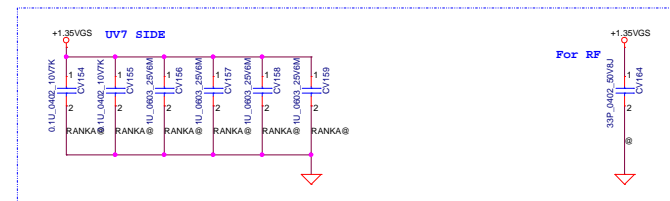
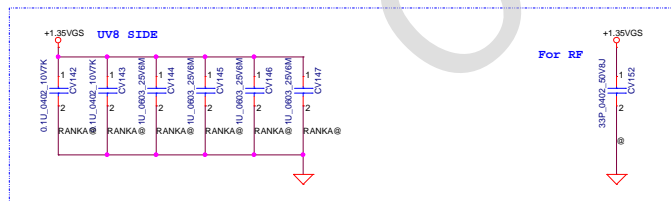
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20 mils spacing to other signals/planes



CMD mapping mod Mode E

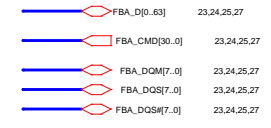
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Fbx_CMD0	ODT_L		ODT_L	
Fbx_CMD1			CS1#_L	
Fbx_CMD2	CS0#_L			
Fbx_CMD3	CKE_L		CKE_L	
Fbx_CMD4	A9	A9	A11	A11
Fbx_CMD5	A6	A6	A7	A7
Fbx_CMD6	A3	A3	BA1	BA1
Fbx_CMD7	A0	A0	A12	A12
Fbx_CMD8	A8	A8	A8	A8
Fbx_CMD9	A12	A12	A0	A0
Fbx_CMD10	A1	A1	A2	A2
Fbx_CMD11	RAS#	RAS#	RAS#	RAS#
Fbx_CMD12	A13	A13	A14	A14
Fbx_CMD13	BA1	BA1	A3	A3
Fbx_CMD14	A14	A14	A13	A13
Fbx_CMD15	CAS#	CAS#	CAS#	CAS#
Fbx_CMD16		ODT_H		ODT_H
Fbx_CMD17			CS1#_H	
Fbx_CMD18		CS0#_H		
Fbx_CMD19		CKE_H		CKE_H
Fbx_CMD20	RST	RST	RST	RST
Fbx_CMD21	A7	A7	A6	A6
Fbx_CMD22	A4	A4	A5	A5
Fbx_CMD23	A11	A11	A9	A9
Fbx_CMD24	A2	A2	A1	A1
Fbx_CMD25	A10	A10	WE#	WE#
Fbx_CMD26	A5	A5	A4	A4
Fbx_CMD27	BA2	BA2		
Fbx_CMD28	WE#	WE#	A10	A10
Fbx_CMD29	BA0	BA0	BA0	BA0
Fbx_CMD30			BA2	BA2



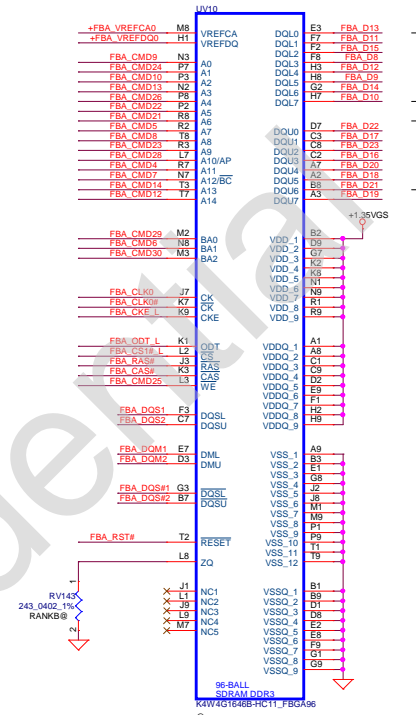
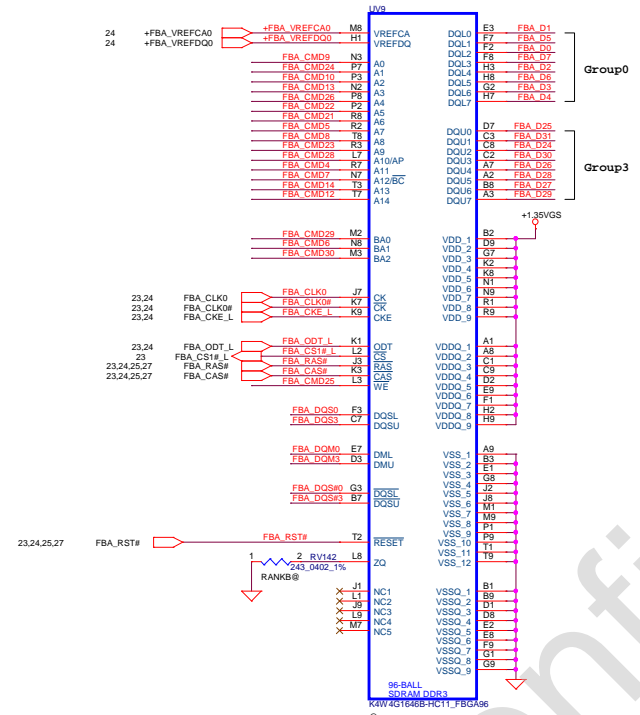
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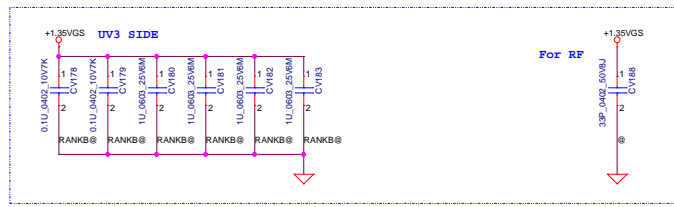
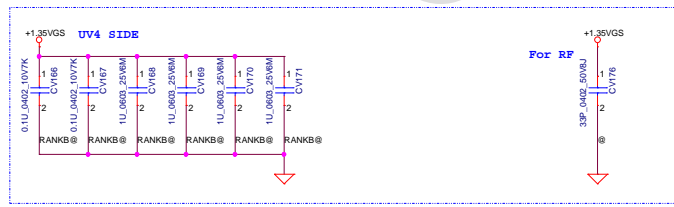


at least 16 mils width (optimal)
20 mils spacing to other signals / planes



CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3			CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

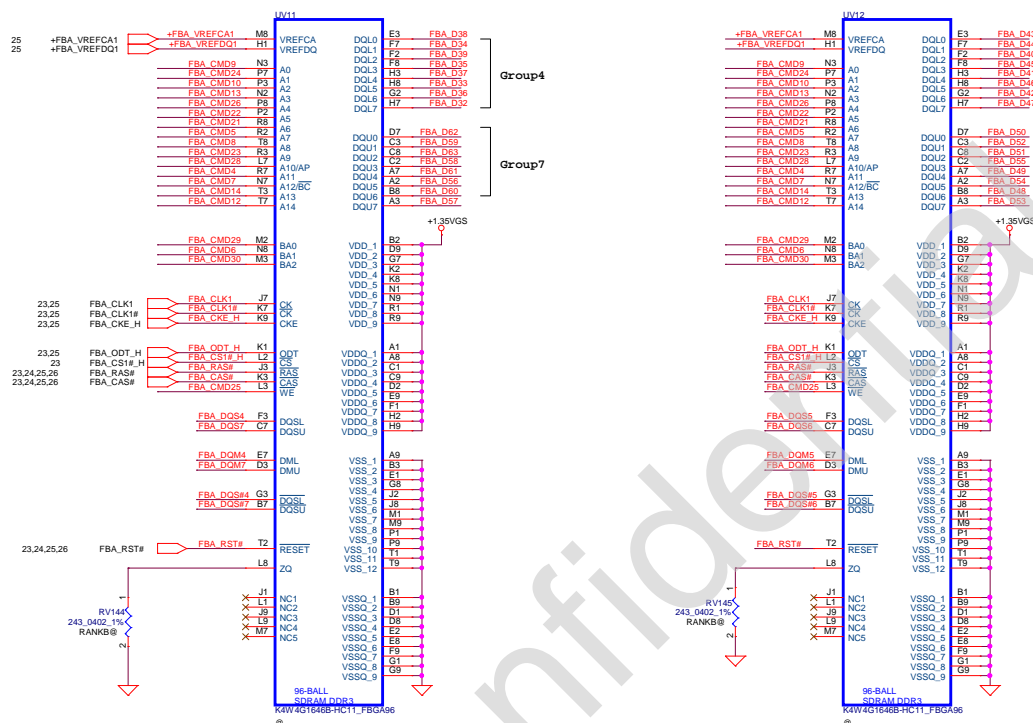


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Title: DDR3 VRAM Rank1_L
 Document Number: AC10A
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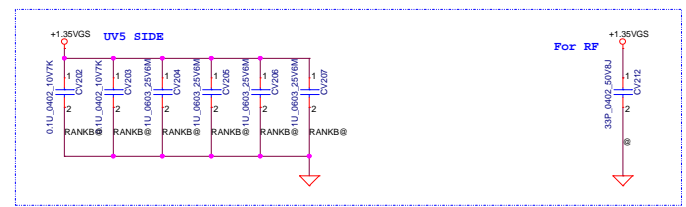
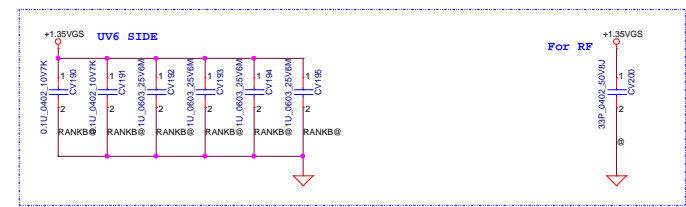
- FBA_D0[0..63] 23.24.25.26
- FBA_CMD[30..0] 23.24.25.26
- FBA_DOM[7..0] 23.24.25.26
- FBA_DQS[7..0] 23.24.25.26
- FBA_DQS[7..0] 23.24.25.26

at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode E

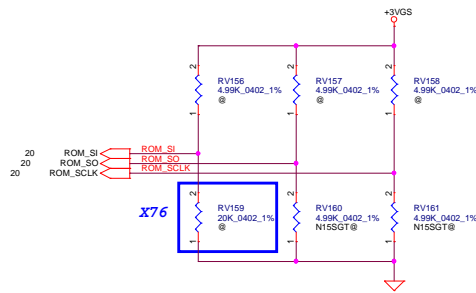
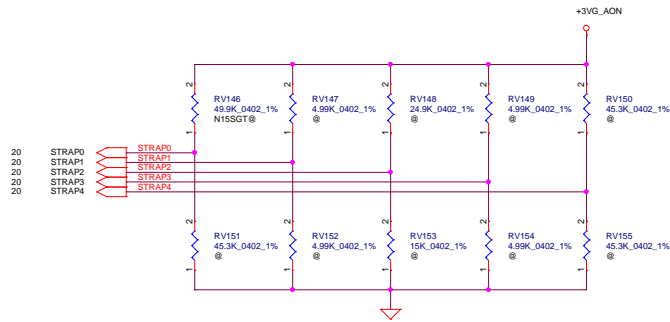
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
Fbx_CMD0	ODT_L		ODT_L	
Fbx_CMD1		CS1#_L		
Fbx_CMD2	CS0#_L			
Fbx_CMD3			CKE_L	
Fbx_CMD4	A9	A9	A11	A11
Fbx_CMD5	A6	A6	A7	A7
Fbx_CMD6	A3	A3	BA1	BA1
Fbx_CMD7	A0	A0	A12	A12
Fbx_CMD8	A8	A8	A8	A8
Fbx_CMD9	A12	A12	A0	A0
Fbx_CMD10	A1	A1	A2	A2
Fbx_CMD11	RAS#	RAS#	RAS#	RAS#
Fbx_CMD12	A13	A13	A14	A14
Fbx_CMD13	BA1	BA1	A3	A3
Fbx_CMD14	A14	A14	A13	A13
Fbx_CMD15	CAS#	CAS#	CAS#	CAS#
Fbx_CMD16		ODT_H		ODT_H
Fbx_CMD17			CS1#_H	
Fbx_CMD18		CS0#_H		
Fbx_CMD19		CKE_H		CKE_H
Fbx_CMD20	RST	RST	RST	RST
Fbx_CMD21	A7	A7	A6	A6
Fbx_CMD22	A4	A4	A5	A5
Fbx_CMD23	A11	A11	A9	A9
Fbx_CMD24	A2	A2	A1	A1
Fbx_CMD25	A10	A10	WE#	WE#
Fbx_CMD26	A5	A5	A4	A4
Fbx_CMD27	BA2	BA2		
Fbx_CMD28	WE#	WE#	A10	A10
Fbx_CMD29	BA0	BA0	BA0	BA0
Fbx_CMD30			BA2	BA2



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DDR3 VRAM Rank1_H

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP3	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP4	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz H5TC4G63AFR-11C 256M x 16	0x3 PD 20K	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
	Micron 900MHz MT41J7256M16HA-093G:E 256M x 16	0x4 PD 24.9K							
	Samsung 900MHz K4W4G1646D-BC1A 256M x 16	0x5 PD 30.1K							


VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

GPU	FB Memory (DDR3)	STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	H5TC4G63AFR-11C 256M x 16	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	MT41J7256M16HA-093G:E 256M x 16	PU 10K	PU 10K	PD 10K	PU 10K				


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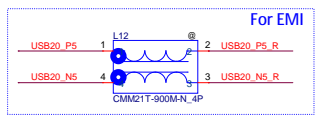
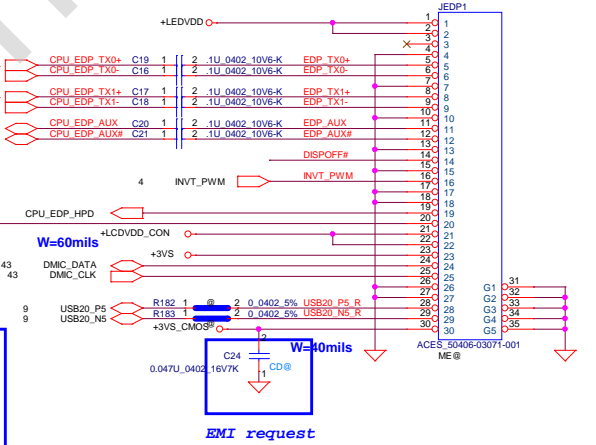
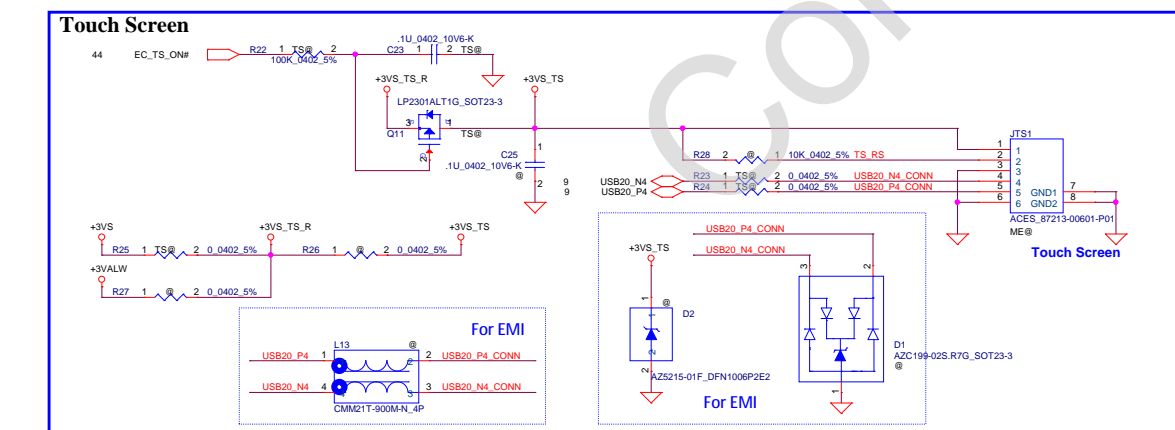
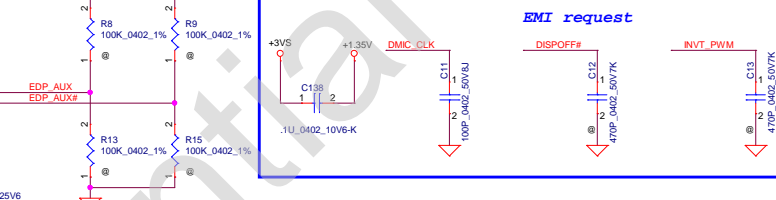
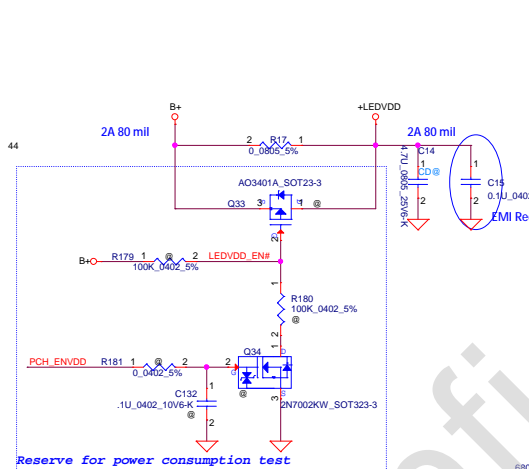
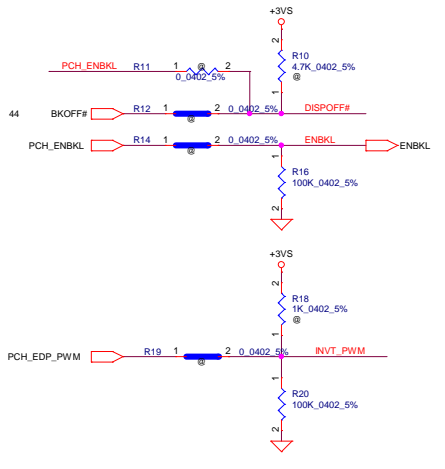
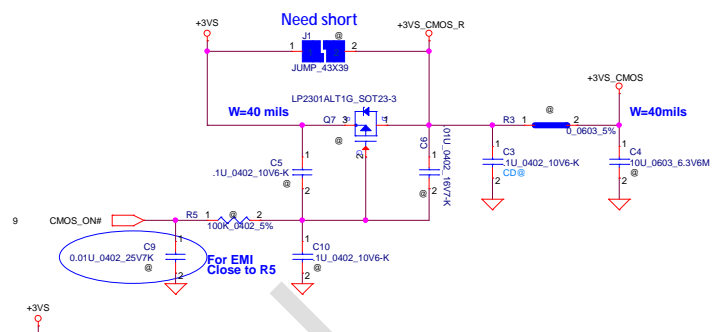
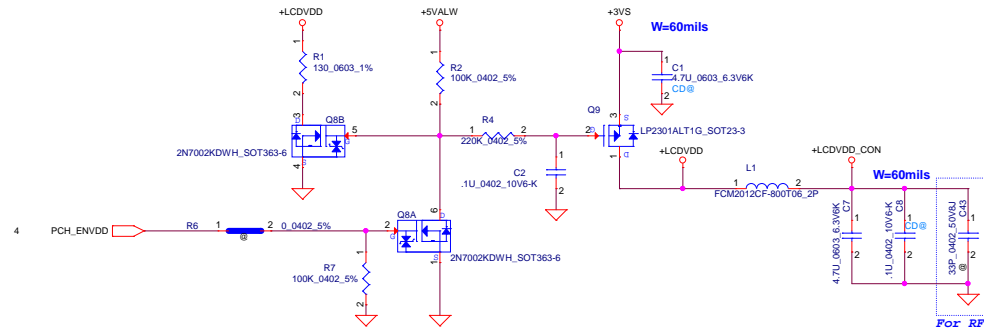
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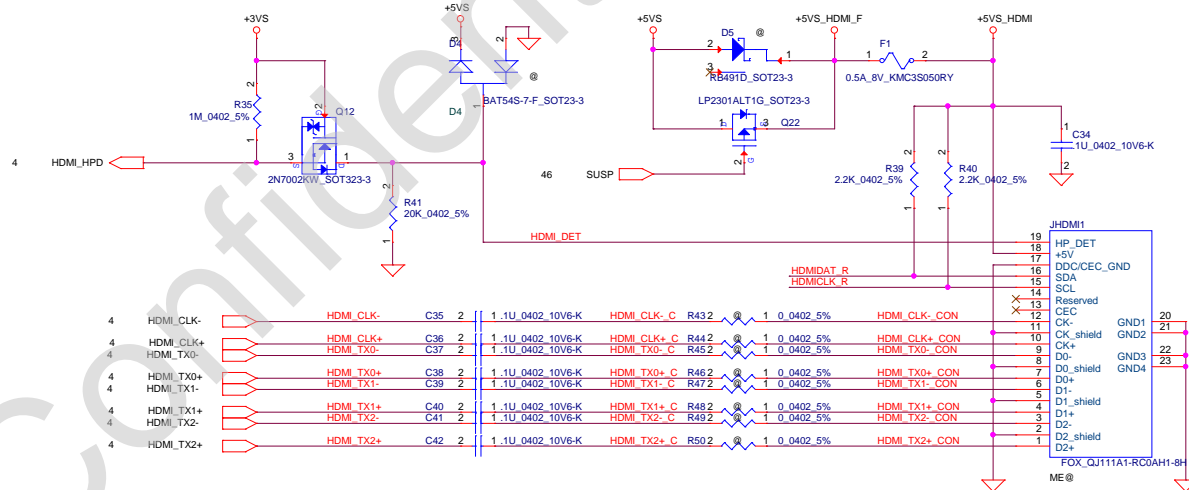
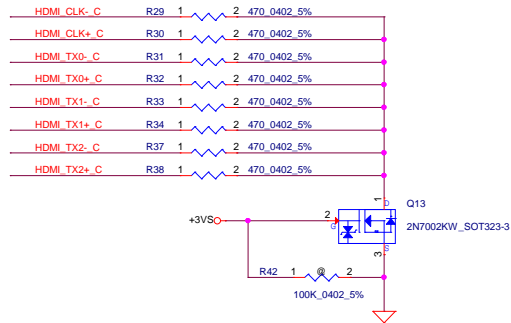
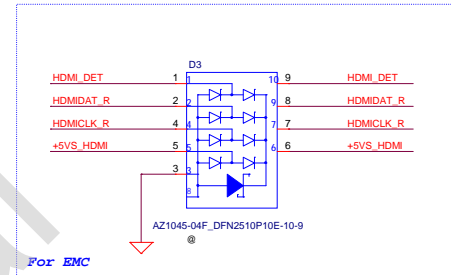
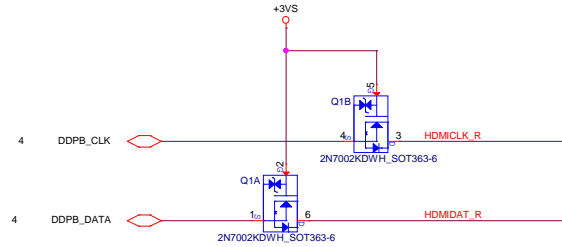
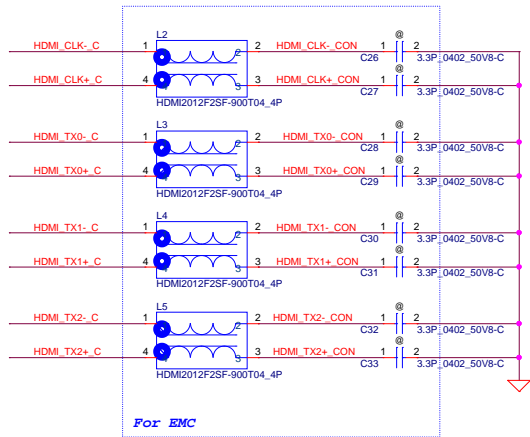
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LCD POWER CIRCUIT

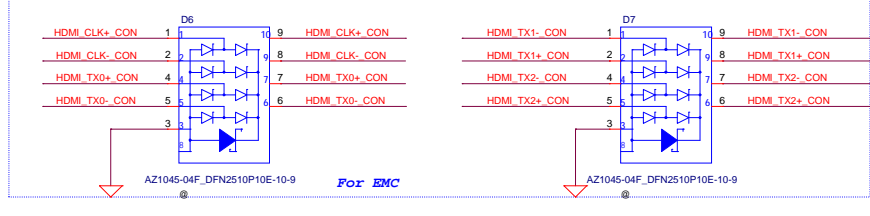
CMOS Camera



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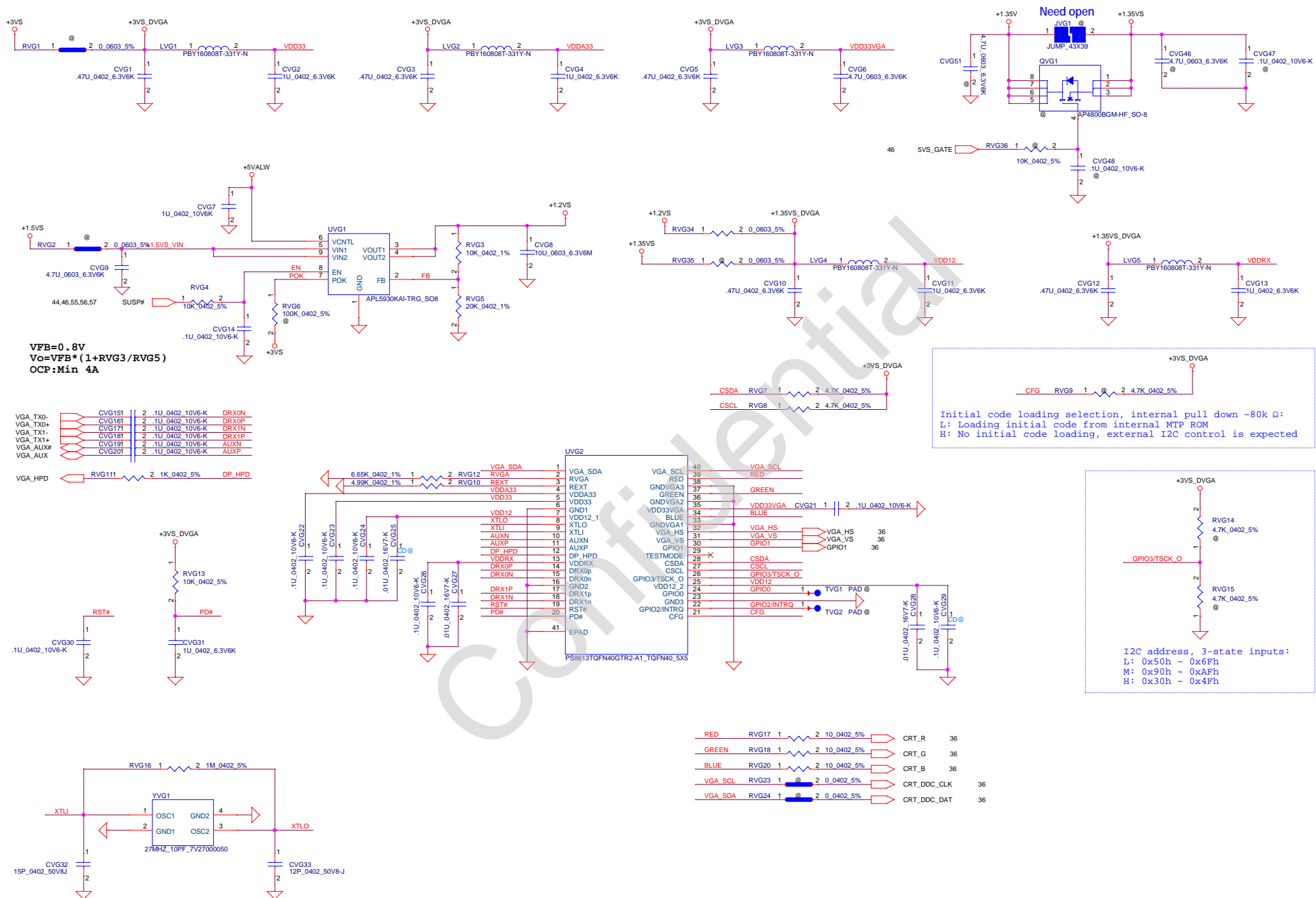


Close to JHDMI1



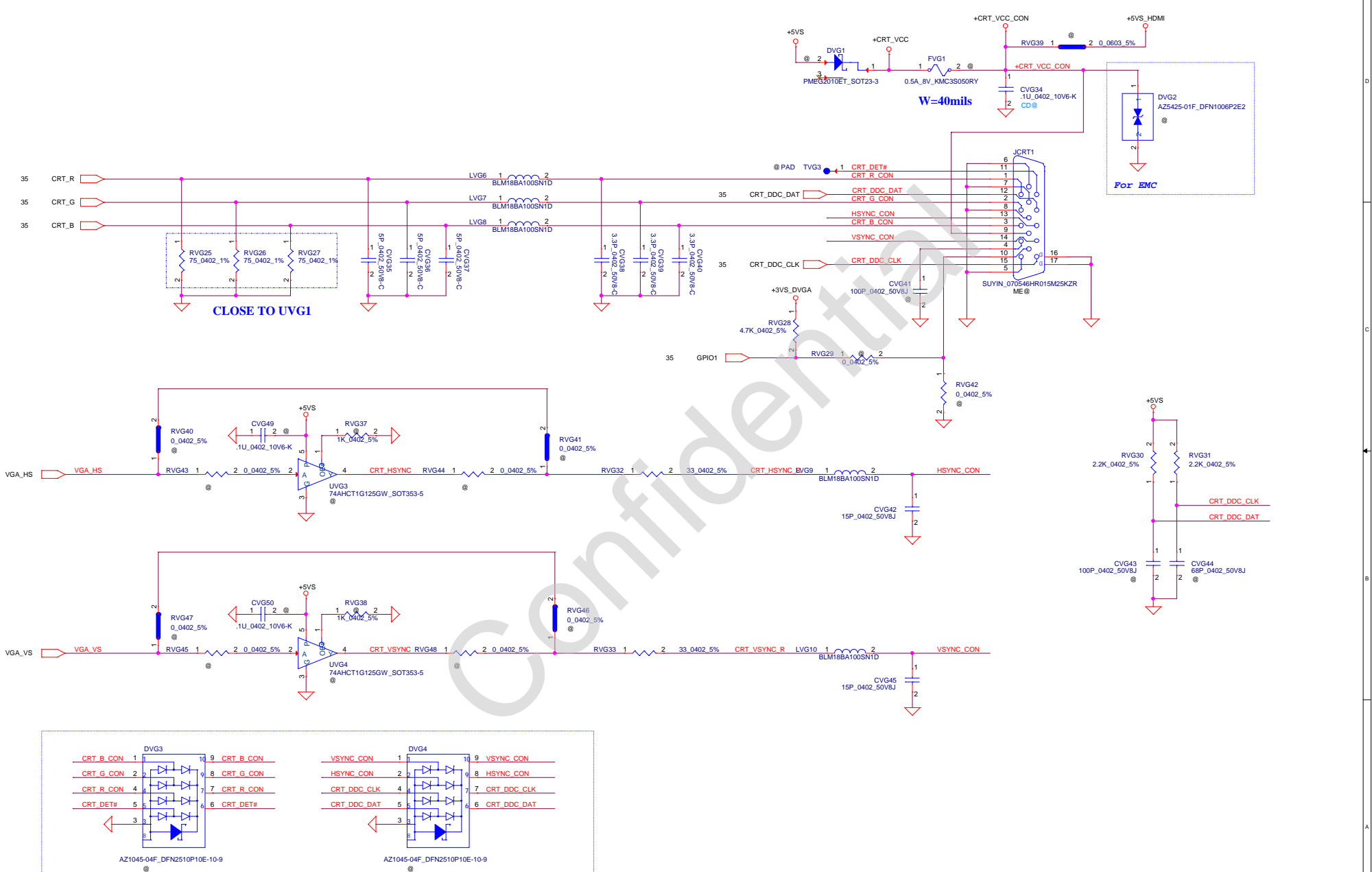
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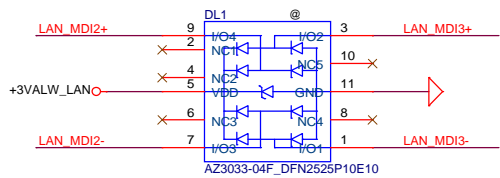
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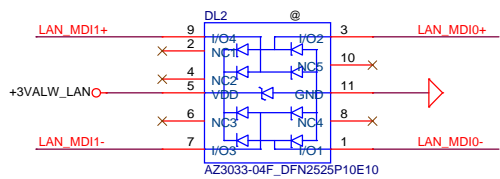
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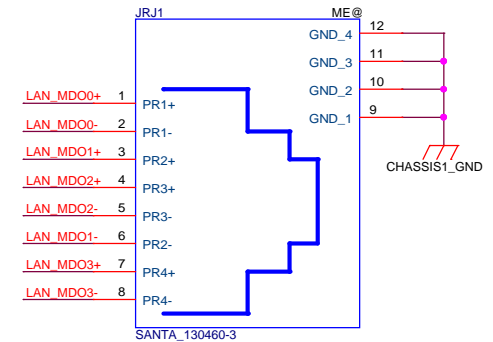
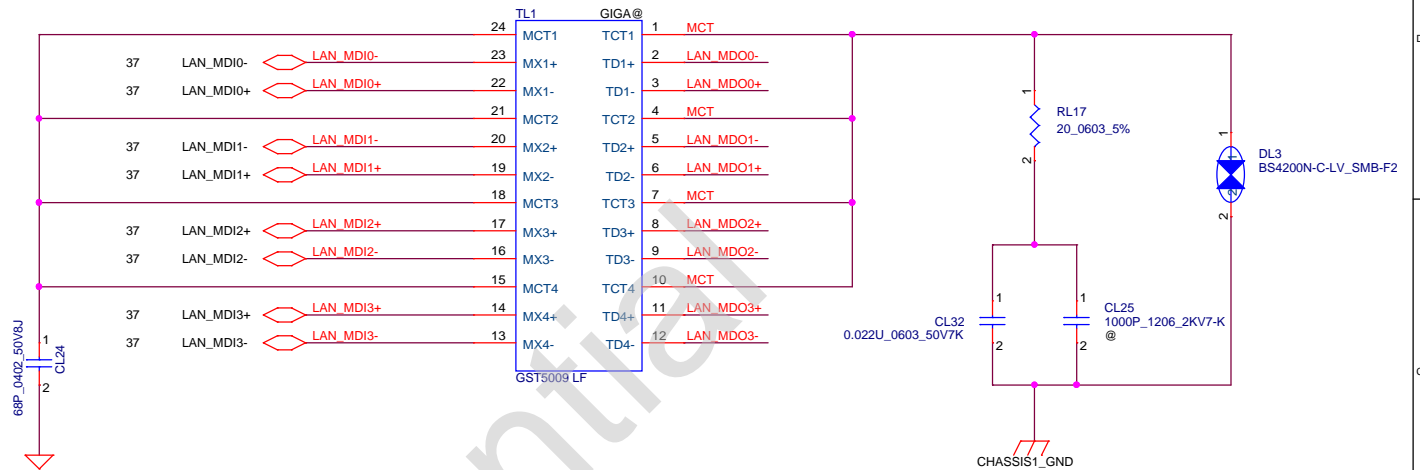
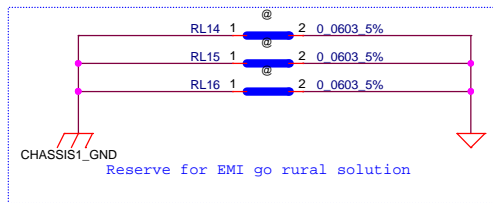
DL1/DL2
1'S PN:SC30003M00



Place Close to TL1

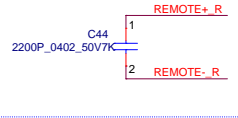


Place Close to TL2

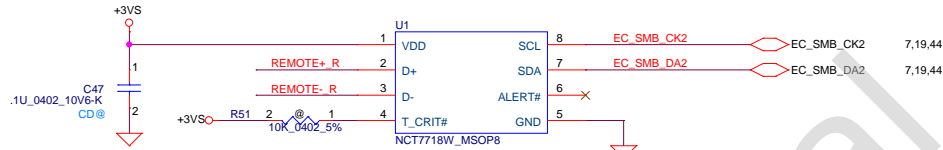


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				Date:	Friday, December 27, 2013

Close to U1



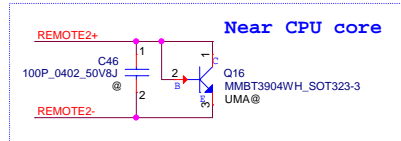
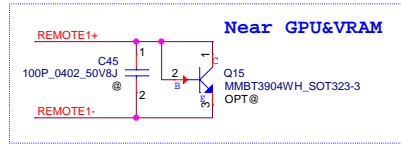
SMSC thermal sensor placed near DIMM



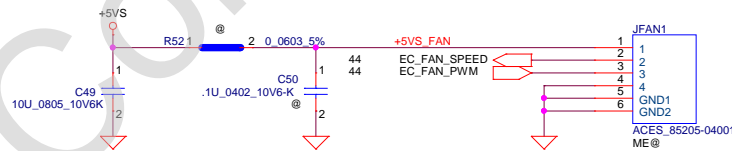
Address 1001_100xb



REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
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Trace length:<8"

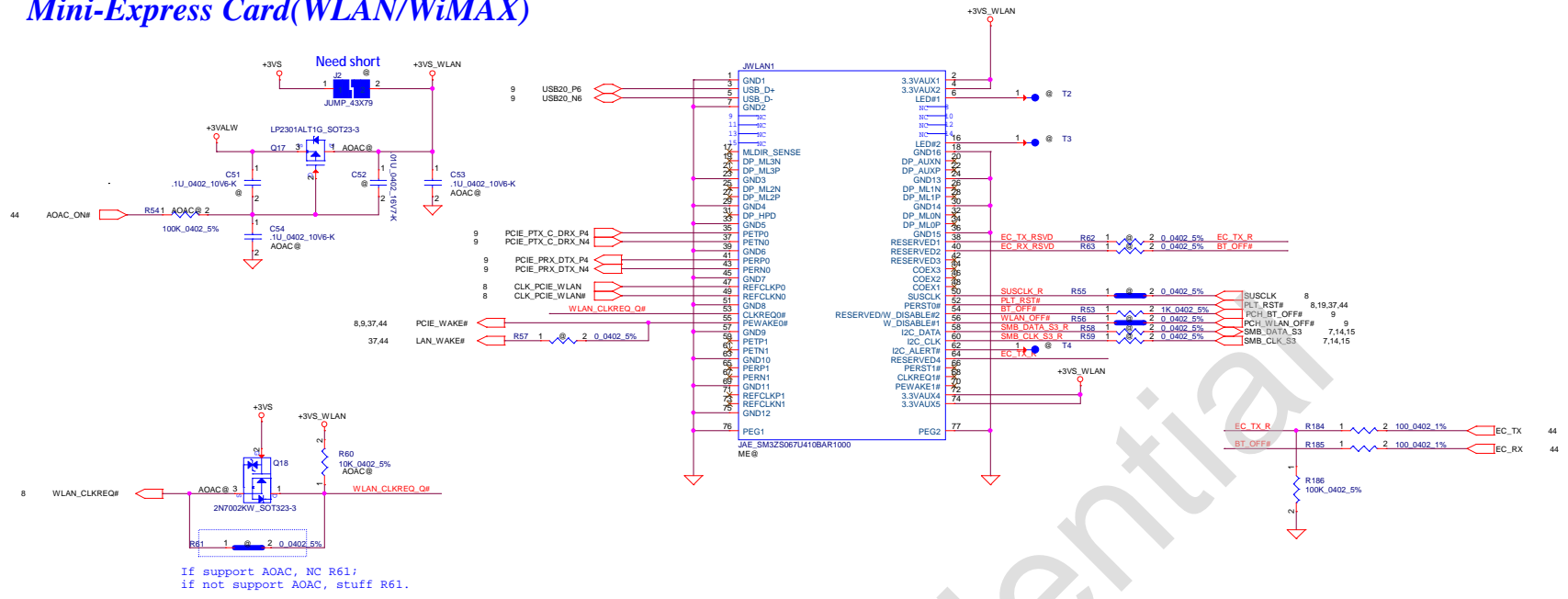


FAN Conn



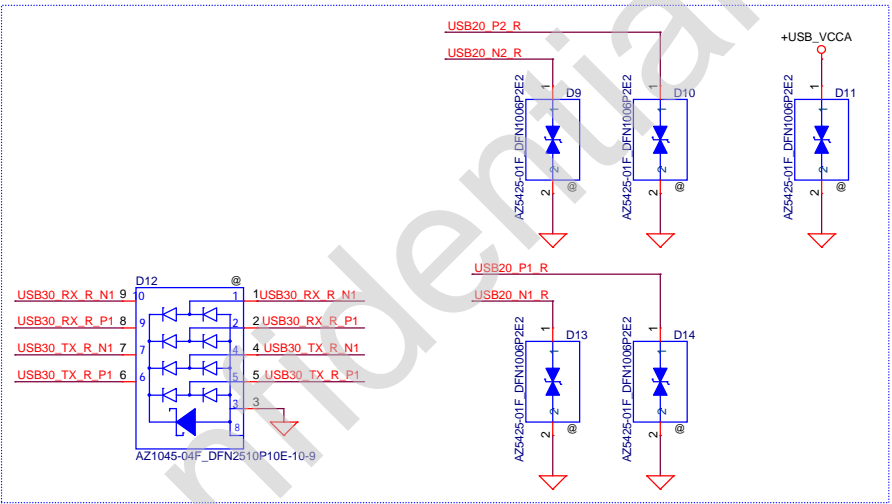
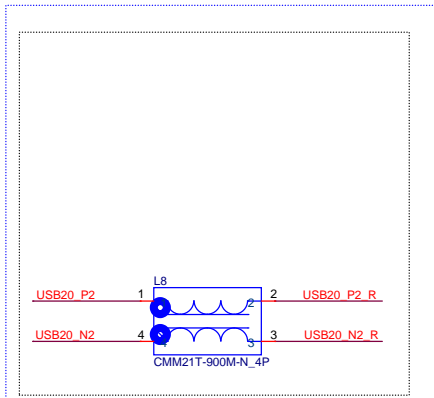
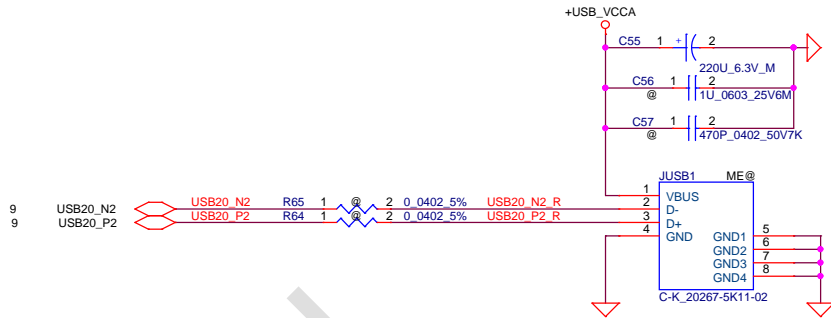
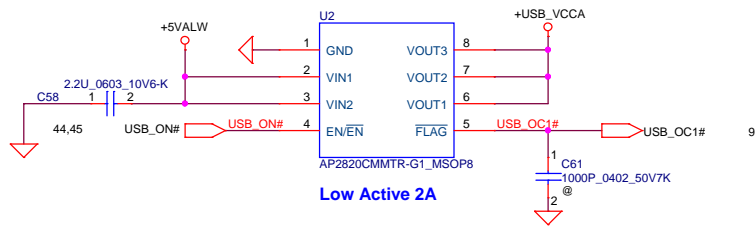
Security Classification	LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05		Thermal sensor/FAN CONN	
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Date:	Thursday, December 26, 2013		Sheet	39	of	59

Mini-Express Card(WLAN/WiMAX)

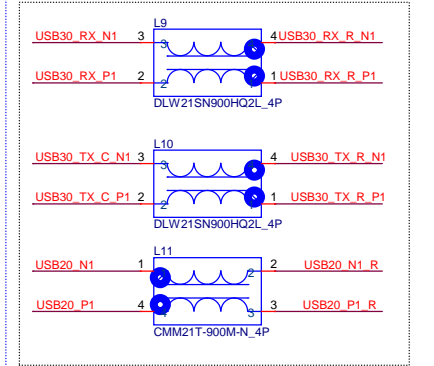


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	NGFF WLAN	
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Date	Thursday, December 26, 2013	Sheet	40	of 59	

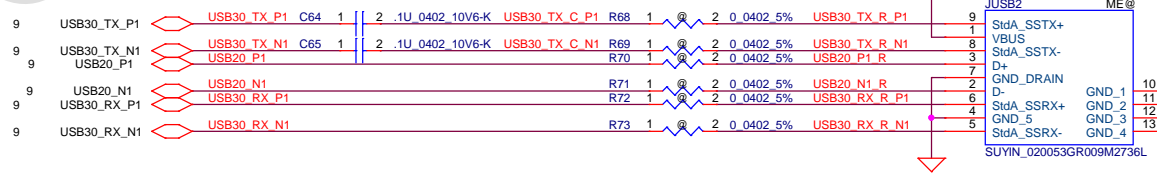
LEFT SIDE USB3.0 PORT X2



For EMC

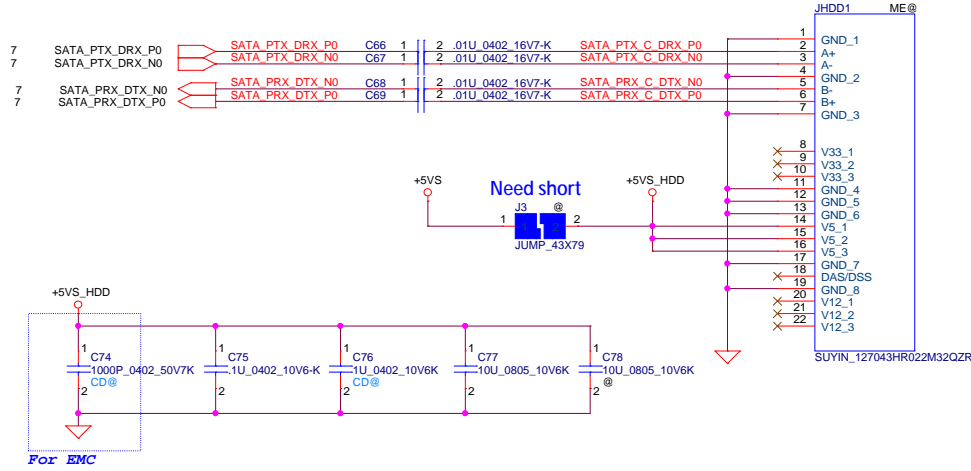


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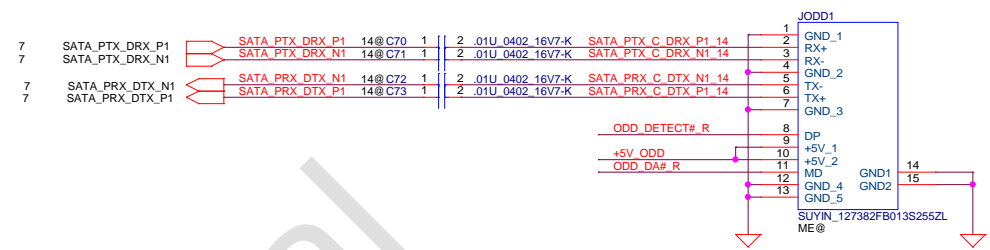


Security Classification		LC Future Center Secret Data		Title	
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Size	Document Number	Date		Thursday, December 26, 2013	Sheet 41 of 59
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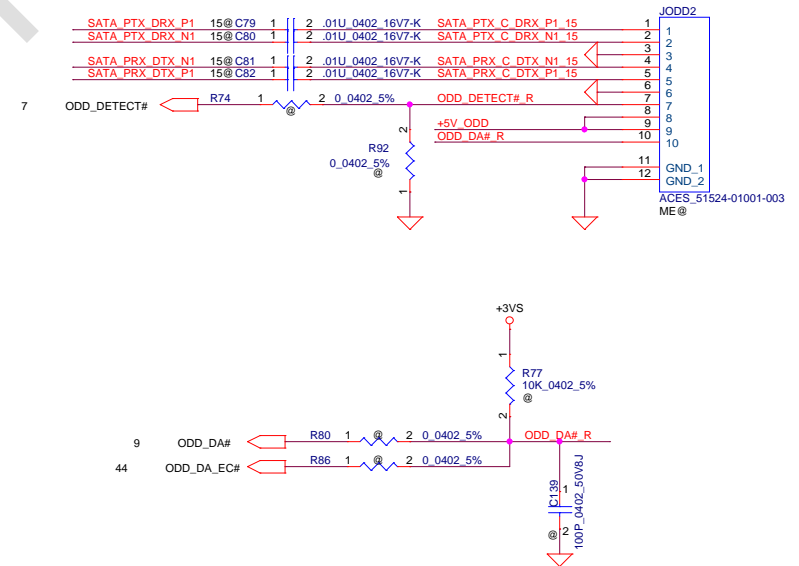
SATA HDD Conn.



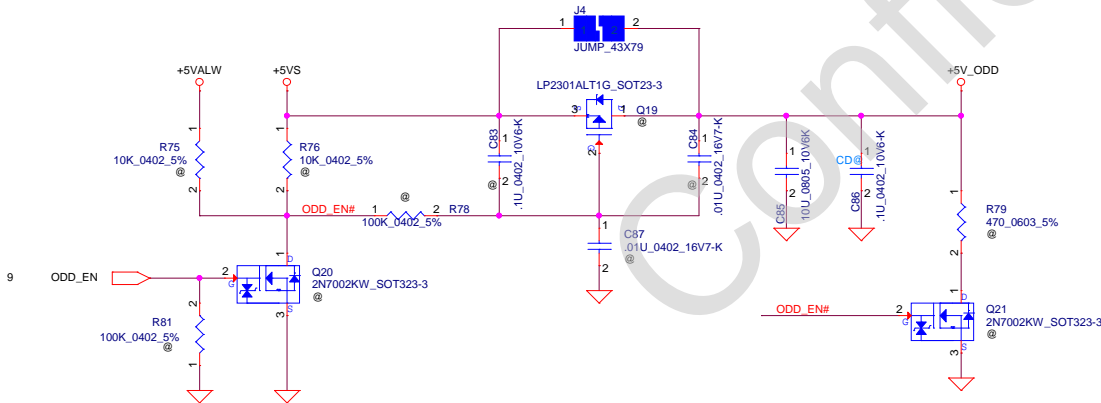
FOR 14" SATA ODD Conn.



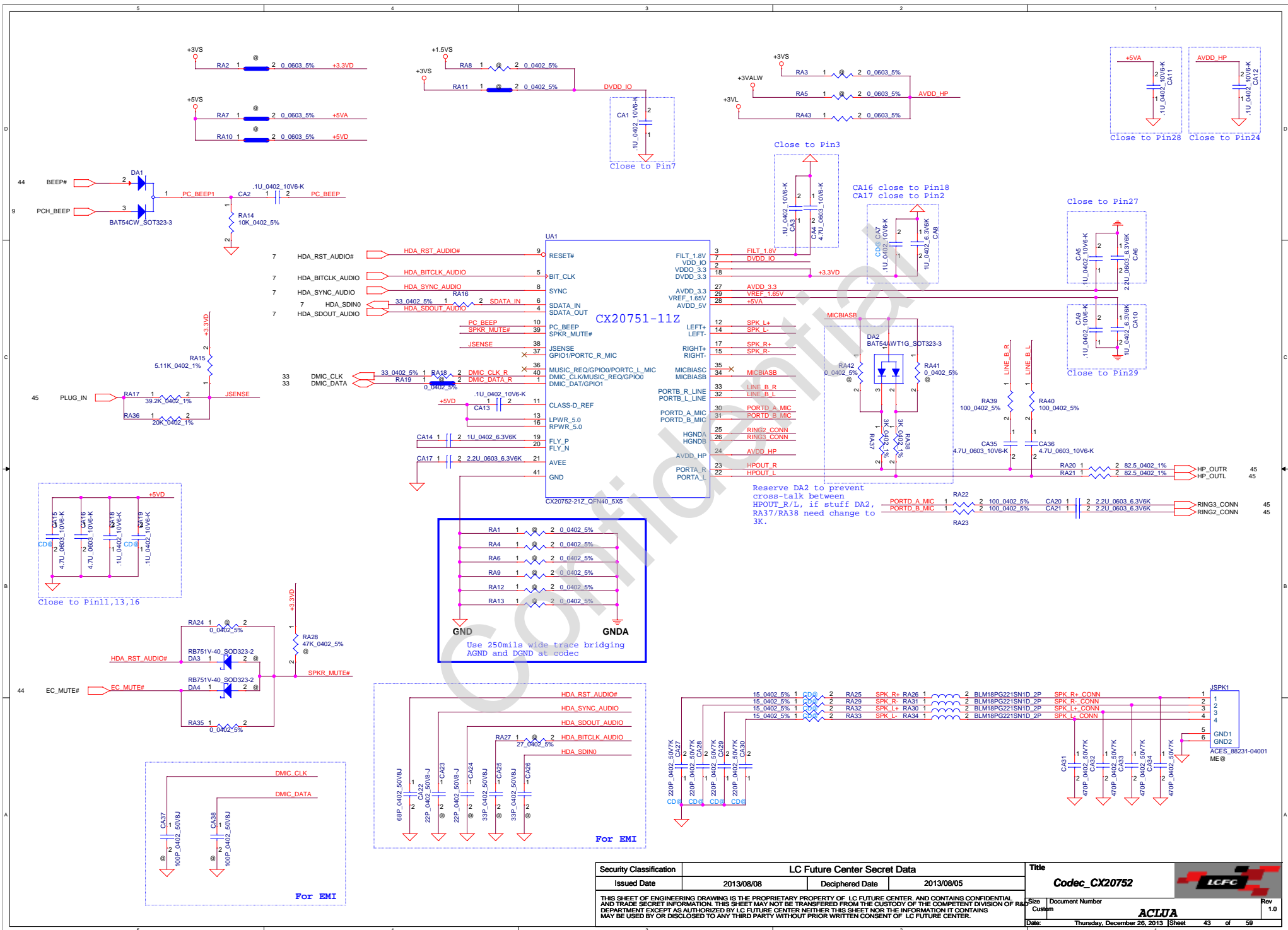
FOR 15" SATA ODD FFC Conn



Need open



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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Size	Document Number	Rev	1.0	
Custom	ACLUA			
Date:	Thursday, December 26, 2013	Sheet	42	of 59



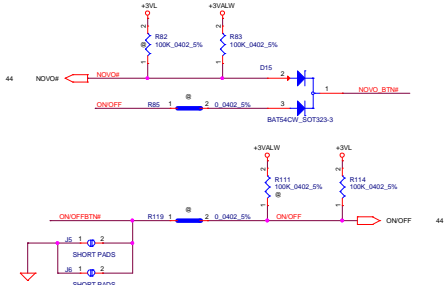
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Codec_CX20752		Document Number	Custom
Date:	Thursday, December 26, 2013	Sheet	43 of 59



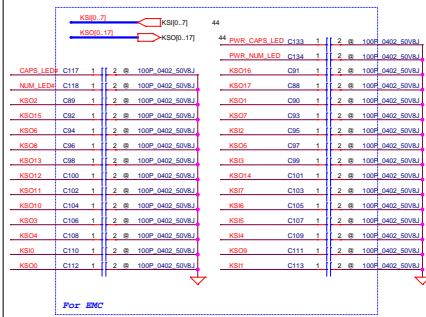
ACES_88231-04001 ME@

ON/OFF switch



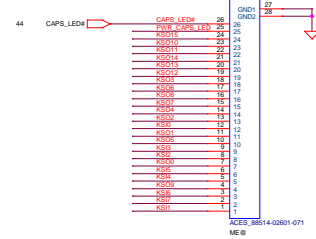
TP/B Connector

K/B Connector

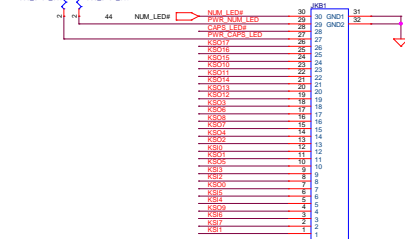


For EMC

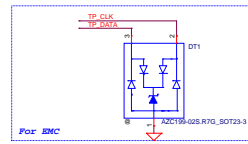
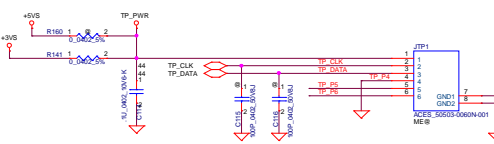
14"



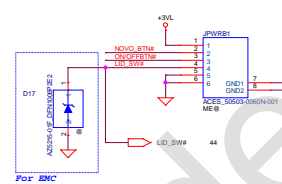
15"



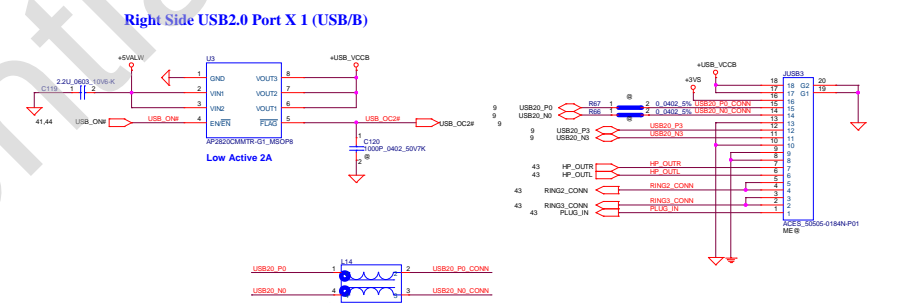
	14"	15"
KB_1	KB14_14	KB09_15
KB_2	KB17_14	KB12_15
KB_3	KB16_14	KB13_15
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KB_5	KB14_14	KB01_15
KB_6	KB15_14	KB10_15
KB_7	KB06_14	KB02_15
KB_8	KB12_14	KB04_15
KB_9	KB13_14	KB07_15
KB_10	KB05_14	KB08_15
KB_11	KB01_14	KB06_15
KB_12	KB10_14	KB03_15
KB_13	KB02_14	KB012_15
KB_14	KB04_14	KB03_15
KB_15	KB07_14	KB04_15
KB_16	KB08_14	KB01_14
KB_17	KB06_14	KB010_15
KB_18	KB03_14	KB015_15
KB_19	KB012_14	KB016_15
KB_20	KB01_14	KB017_15
KB_21	KB04_14	KB_LRD_PWR_5
KB_22	KB011_14	CAPS_LEDH_5
KB_23	KB010_14	VDD_15
KB_24	KB015_14	NIM_LEDH_15



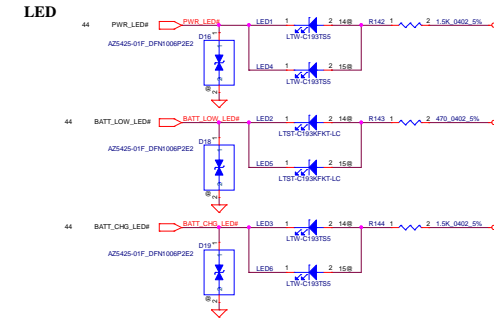
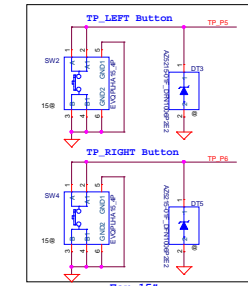
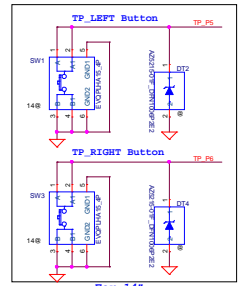
PWR/B Connector



USB I/O Connector

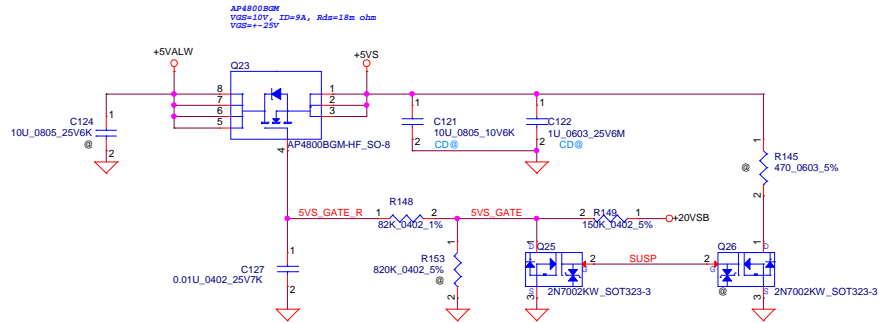


For 14"	For 15"
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

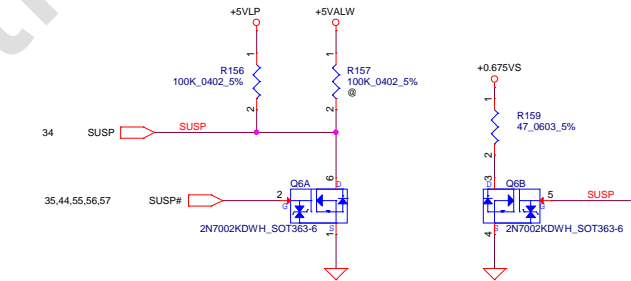
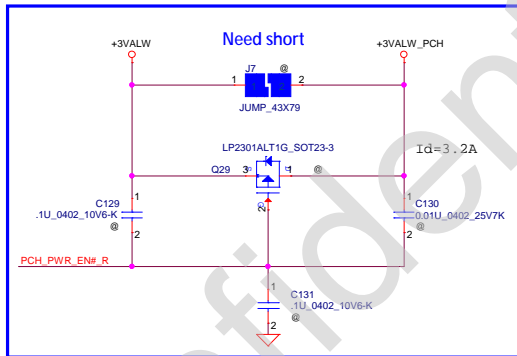
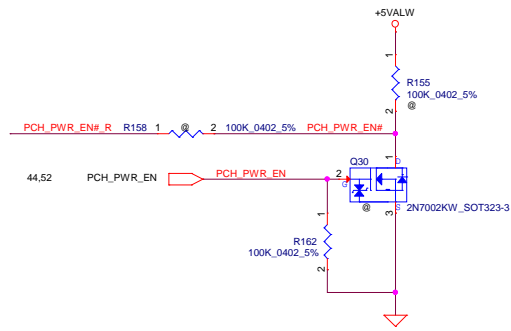
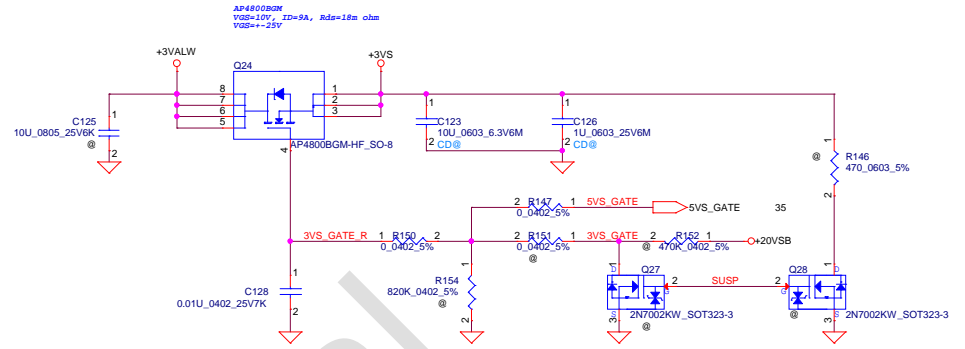


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	KBD/PWR/OLED/TP Conn.		Rev		1.0	
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+5VALW to +5VS

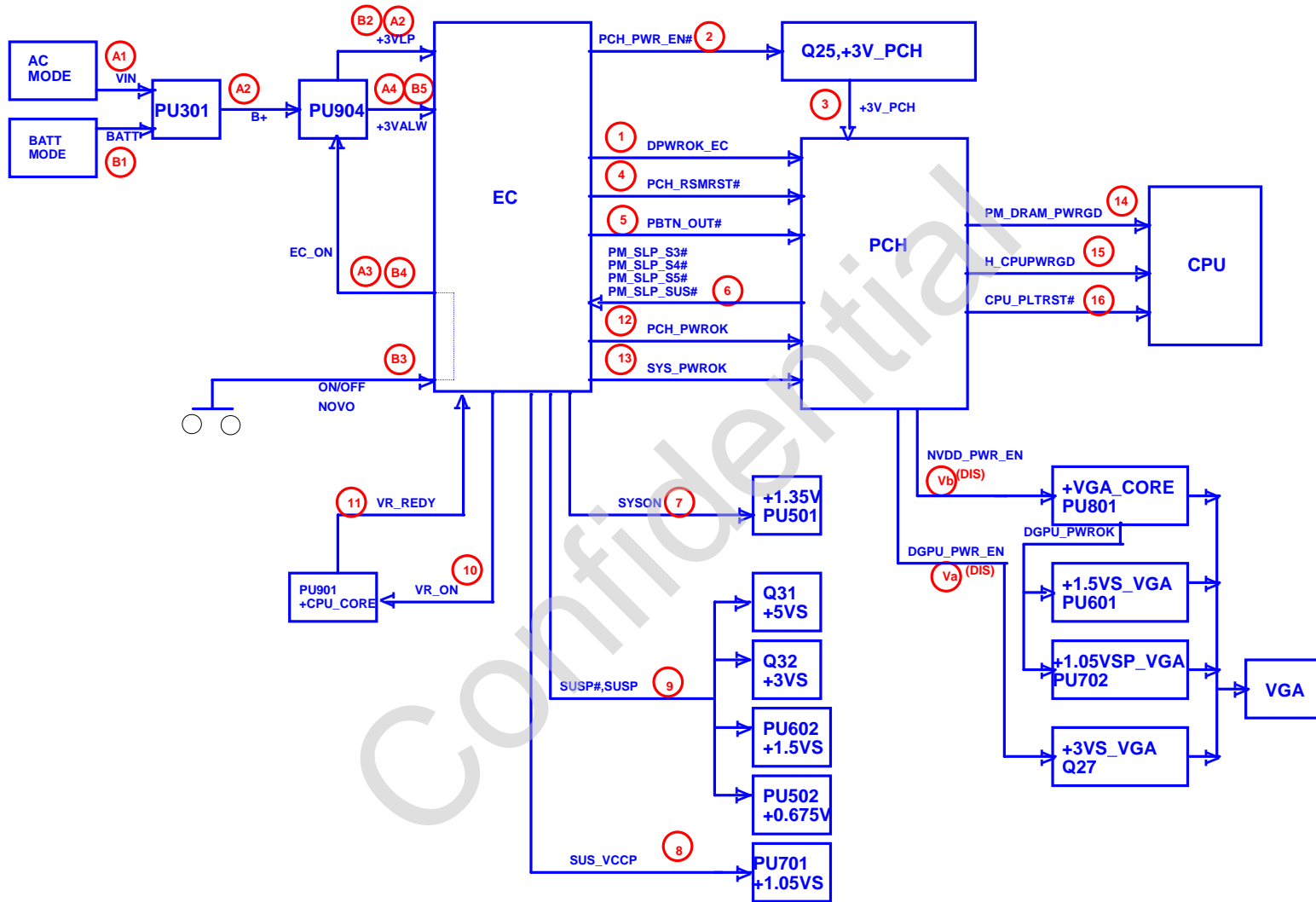


+3VALW to +3VS




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		2013/08/05
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Title		
Power sequence Block		
Size	Document Number	Rev
Custom		1.0
Date: Thursday, December 26, 2013 [Sheet 47 of 59]		

LAN chip

UL1 100M@
RTL8106EUL-CG
SA00006000

Transformer

TL1 100M@
TST1284A LF
SP00008C00

X76 BOM

ZZZ2 H4GX8T@ Hynix X7603212001
 ZZZ3 M4GX8T@ Micron X7603212002
 ZZZ4 H2GX4T@ Hynix X7603212003
 ZZZ5 H2GX4M@ Hynix X7603212051
 ZZZ6 M2GX4M@ Micron X7603212052
 ZZZ7 M2GX4T@ Micron X7603212004
 ZZZ8 S4GX8T@ Samsung X7603212054
 ZZZ9 S2GX4T@ Samsung X7603212053

ZZZ10 14@ PCB PN DA20T00100
 ZZZ11 15@ PCB PN DA20T200100
 PCB_MB

Empty component box

UV1 N15VGM@ NV N15V-GM GPU SA000064R00
 RV155 N15VGM@ 10K 0402 1% SD03410028J
 RV159 N15VGM@ 10K 0402 1% SD03410028J
 RV160 N15VGM@ 10K 0402 1% SD03410028J
 RV161 N15VGM@ 10K 0402 1% SD03410028J

Hynix 4G---256X16 *8 pcs X7603212001

UV5 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV6 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV7 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV8 H4T@ H5TC4G63AFR-11C SA00005YL00
 RC100 H4T@ 10K 0402 5% SD02810028J
 UV9 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV10 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV11 H4T@ H5TC4G63AFR-11C SA00005YL00
 UV12 H4T@ H5TC4G63AFR-11C SA00005YL00
 RV159 H4T@ 20K 0402 1% SD03420028J

Hynix 2G---256X16 *4 pcs X7603212051

UV5 H2M@ H5TC4G63AFR-11C SA00005YL00
 UV6 H2M@ H5TC4G63AFR-11C SA00005YL00
 UV7 H2M@ H5TC4G63AFR-11C SA00005YL00
 UV8 H2M@ H5TC4G63AFR-11C SA00005YL00
 RC107 H2M@ 10K 0402 5% SD02810028J
 RV148 H2M@ 10K 0402 1% SD03410028J
 RV151 H2M@ 10K 0402 1% SD03410028J
 RV152 H2M@ 10K 0402 1% SD03410028J
 RV154 H2M@ 10K 0402 1% SD03410028J

Micron 4G---256X16 *8 pcs X7603212002

UV5 M4T@ MT41J256M16HA-093G.E SA00006010
 UV6 M4T@ MT41J256M16HA-093G.E SA00006010
 UV7 M4T@ MT41J256M16HA-093G.E SA00006010
 UV8 M4T@ MT41J256M16HA-093G.E SA00006010
 RC100 M4T@ 10K 0402 5% SD02810028J
 UV9 M4T@ MT41J256M16HA-093G.E SA00006010
 UV10 M4T@ MT41J256M16HA-093G.E SA00006010
 UV11 M4T@ MT41J256M16HA-093G.E SA00006010
 UV12 M4T@ MT41J256M16HA-093G.E SA00006010
 RV159 M4T@ 24.9K 0402 1% SD03420028J

Micron 2G---256X16 *4 pcs X7603212052

UV5 M2M@ MT41J256M16HA-093G.E SA00006010
 UV6 M2M@ MT41J256M16HA-093G.E SA00006010
 UV7 M2M@ MT41J256M16HA-093G.E SA00006010
 UV8 M2M@ MT41J256M16HA-093G.E SA00006010
 RC107 M2M@ 10K 0402 5% SD02810028J
 RV148 M2M@ 10K 0402 1% SD03410028J
 RV149 M2M@ 10K 0402 1% SD03410028J
 RV152 M2M@ 10K 0402 1% SD03410028J

Hynix 2G---256X16 *4 pcs X7603212003

UV5 H2T@ H5TC4G63AFR-11C SA00005YL00
 UV6 H2T@ H5TC4G63AFR-11C SA00005YL00
 UV7 H2T@ H5TC4G63AFR-11C SA00005YL00
 UV8 H2T@ H5TC4G63AFR-11C SA00005YL00
 RC107 H2T@ 10K 0402 5% SD02810028J
 RV159 H2T@ 20K 0402 1% SD03420028J

Micron 2G---256X16 *4 pcs X7603212004

UV5 M2T@ MT41J256M16HA-093G.E SA00006010
 UV6 M2T@ MT41J256M16HA-093G.E SA00006010
 UV7 M2T@ MT41J256M16HA-093G.E SA00006010
 UV8 M2T@ MT41J256M16HA-093G.E SA00006010
 RC107 M2T@ 10K 0402 5% SD02810028J
 RV159 M2T@ 24.9K 0402 1% SD03420028J

Samsung 4G---256X16 *8 pcs X7603212054

UV5 S4T@ K4W4G1646D-BC1A SA000063F10
 UV6 S4T@ K4W4G1646D-BC1A SA000063F10
 UV7 S4T@ K4W4G1646D-BC1A SA000063F10
 UV8 S4T@ K4W4G1646D-BC1A SA000063F10
 RC100 S4T@ 10K 0402 5% SD02810028J
 UV9 S4T@ K4W4G1646D-BC1A SA000063F10
 UV10 S4T@ K4W4G1646D-BC1A SA000063F10
 UV11 S4T@ K4W4G1646D-BC1A SA000063F10
 UV12 S4T@ K4W4G1646D-BC1A SA000063F10
 RV159 S4T@ 30.1K 0402 1% SD03430128J

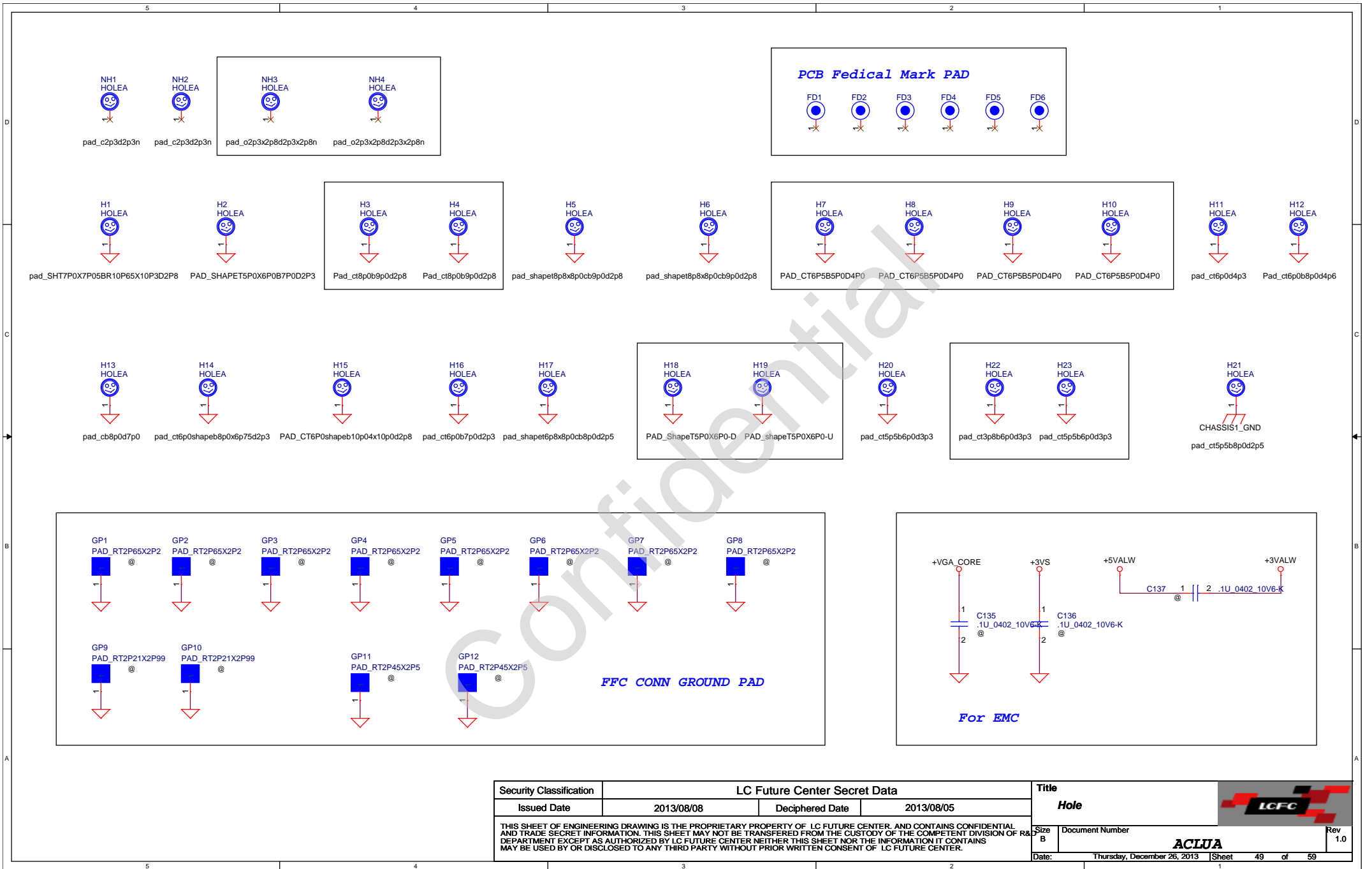
Samsung 2G---256X16 *4 pcs X7603212053

UV5 S2T@ K4W4G1646D-BC1A SA000063F10
 UV6 S2T@ K4W4G1646D-BC1A SA000063F10
 UV7 S2T@ K4W4G1646D-BC1A SA000063F10
 UV8 S2T@ K4W4G1646D-BC1A SA000063F10
 RC107 S2T@ 10K 0402 5% SD02810028J
 RV159 S2T@ 30.1K 0402 1% SD03430128J

PR9440 27K 0402 1% N15VGM@
 PR9434 7.5K 0402 1% N15VGM@
 PR9436 0.0402 5% N15VGM@
 PR9437 6.2K 0402 1% N15VGM@
 PR9431 1.7K 0402 1% N15VGM@
 PC1277 5600P 0402 25V7-K N15VGM@

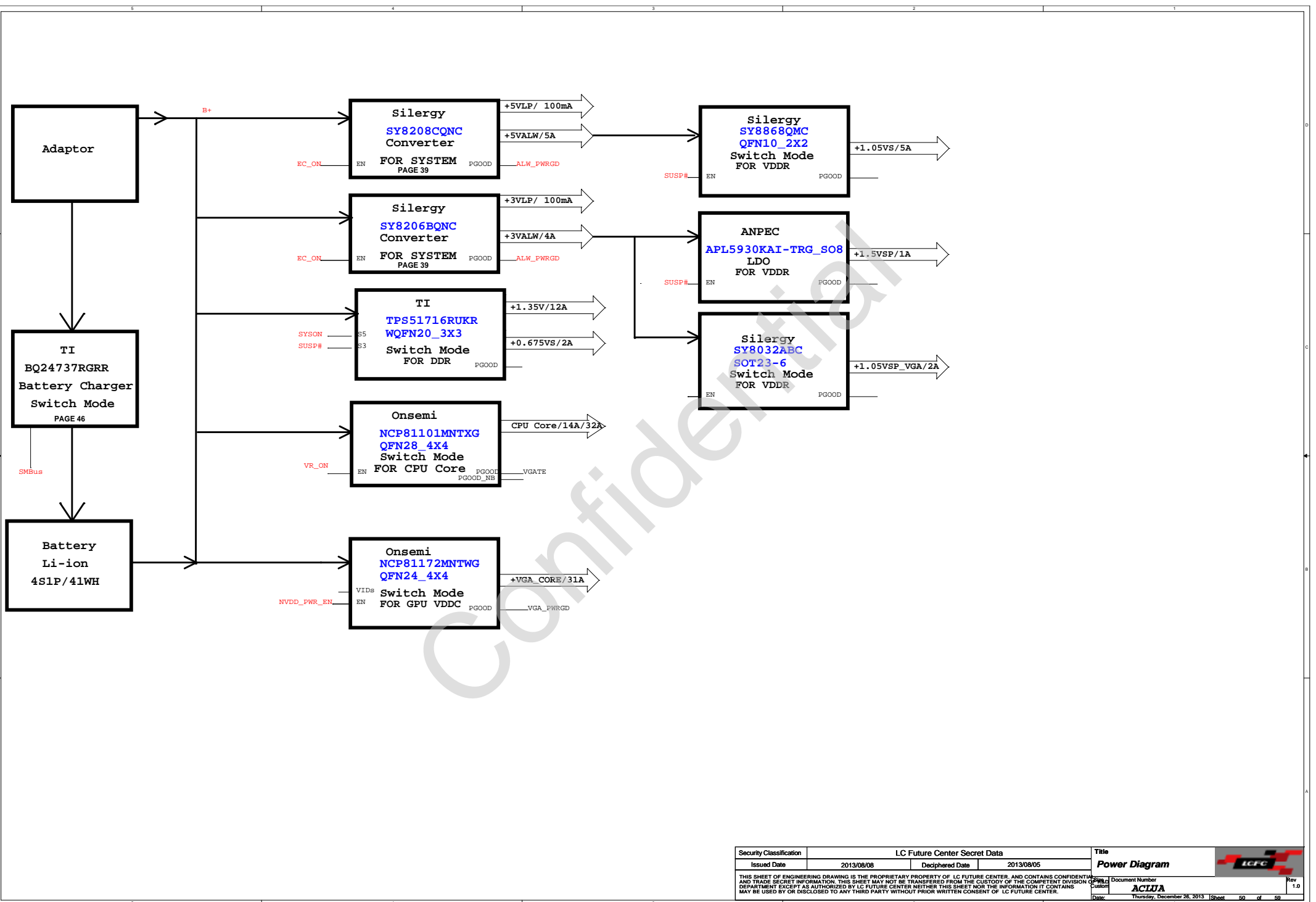
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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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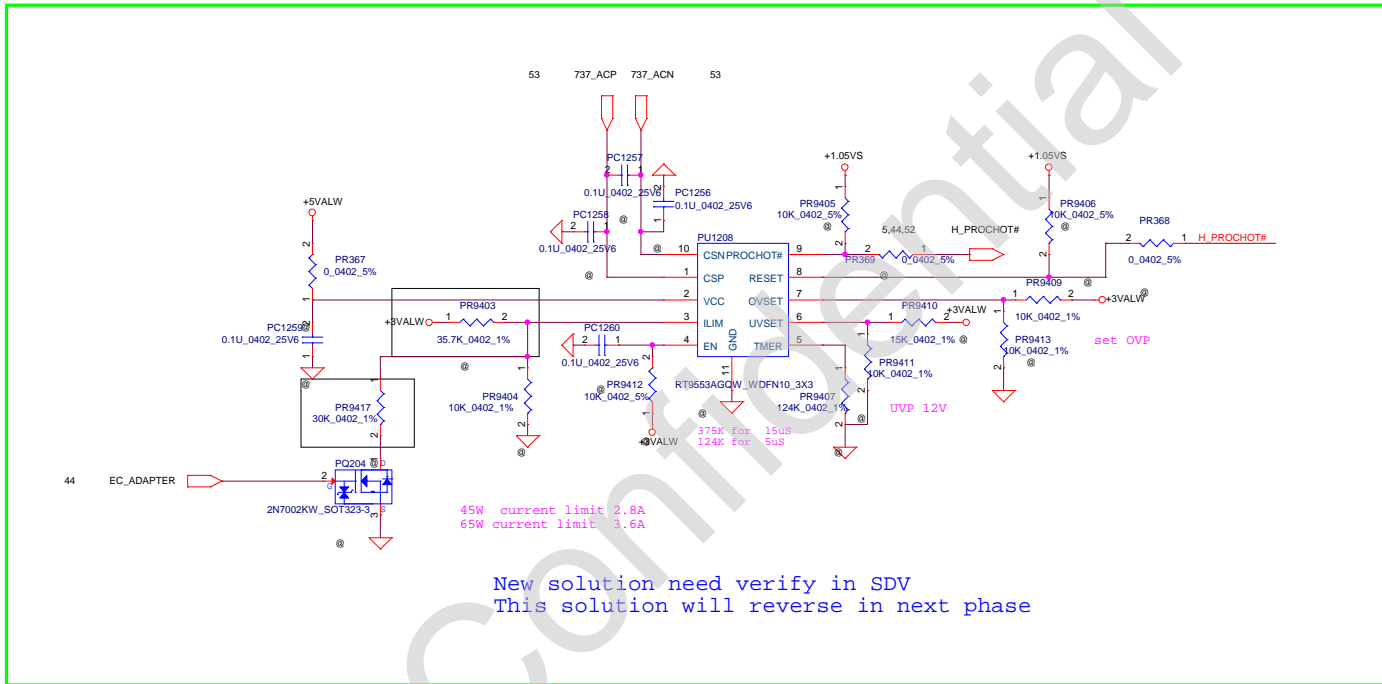
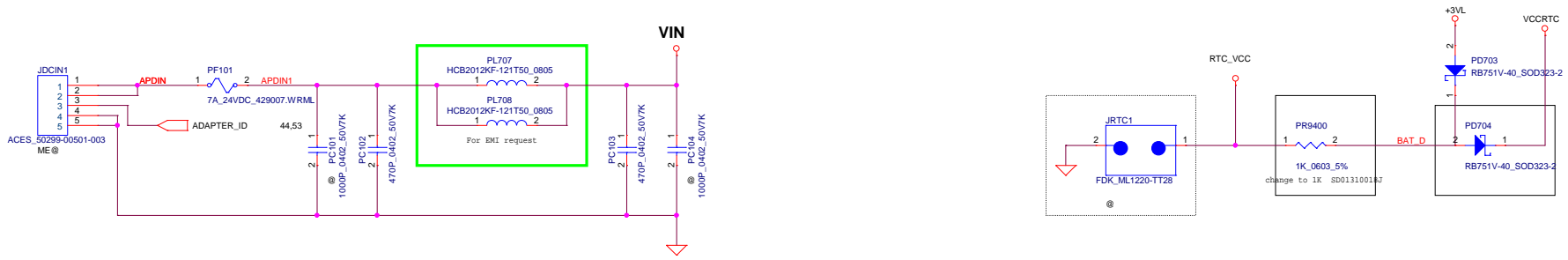


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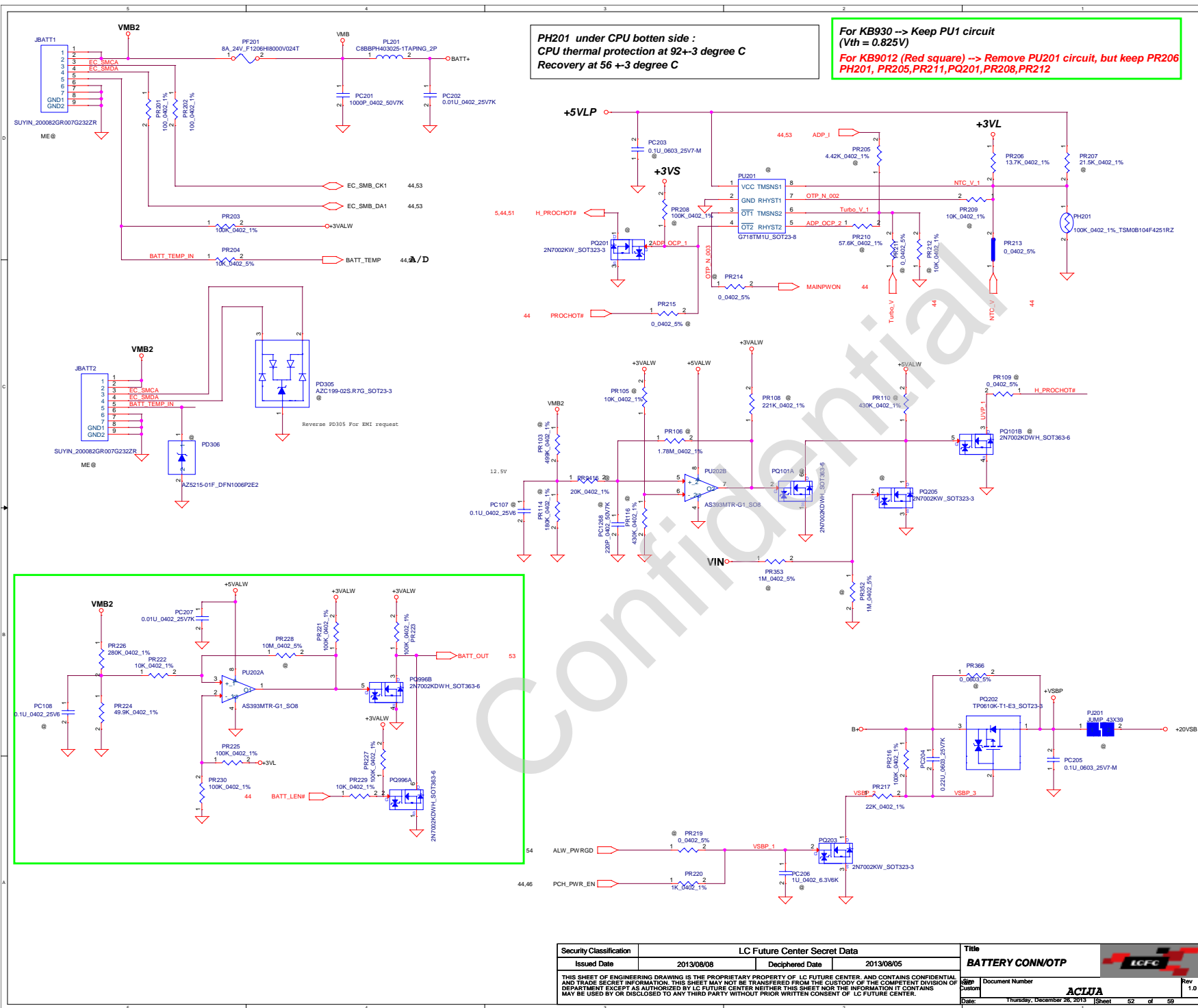
New solution need verify in SDV
 This solution will reverse in next phase

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		2013/08/05
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ACLUJA



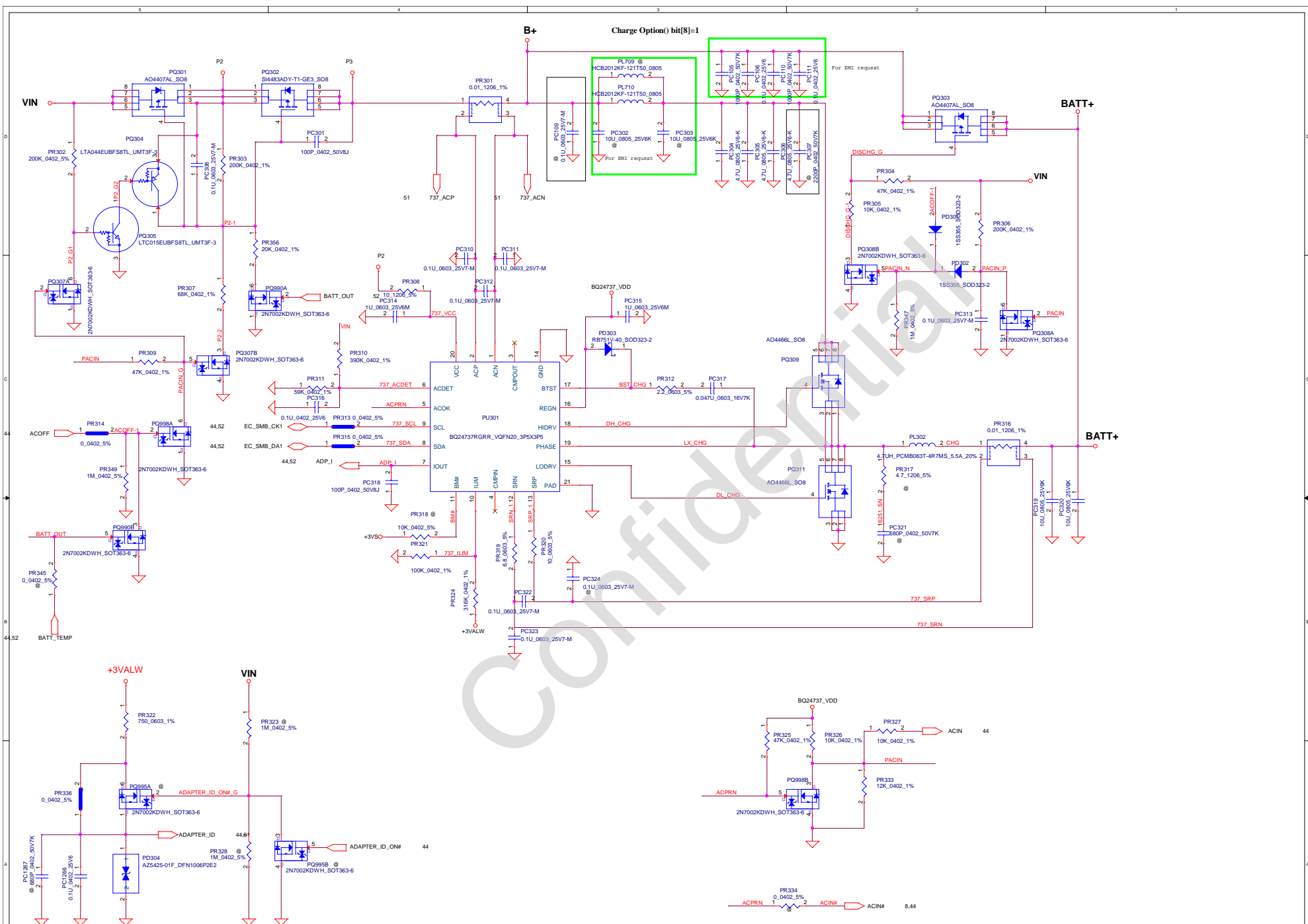
PH201 under CPU bottom side :
 CPU thermal protection at 92+3 degree C
 Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit
 (Vth = 0.825V)
 For KB912 (Red square) --> Remove PU201 circuit, but keep PR206
 PH201, PR205, PR211, PQ201, PR208, PR212

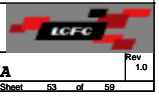
Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date
		2013/08/05

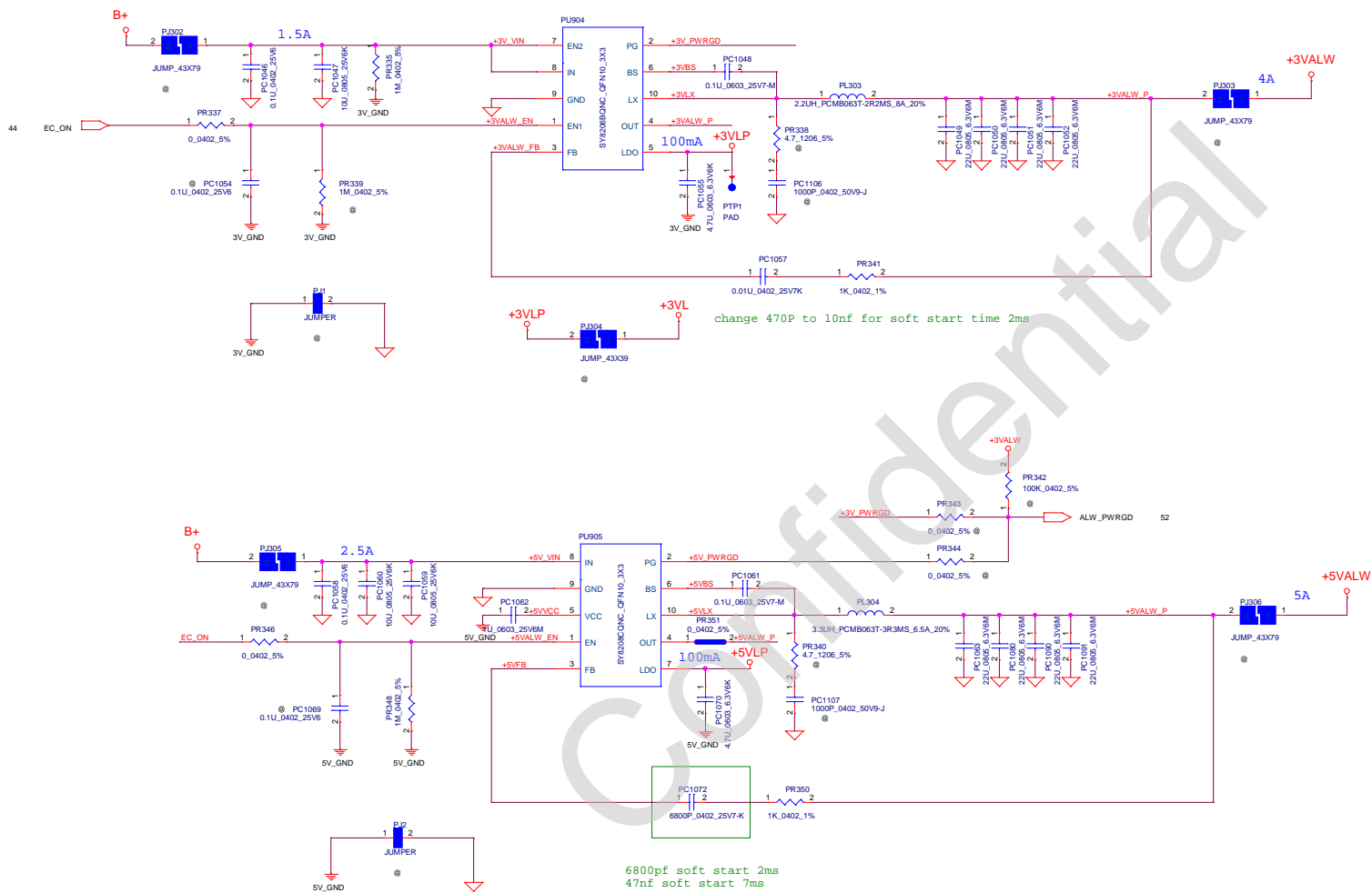
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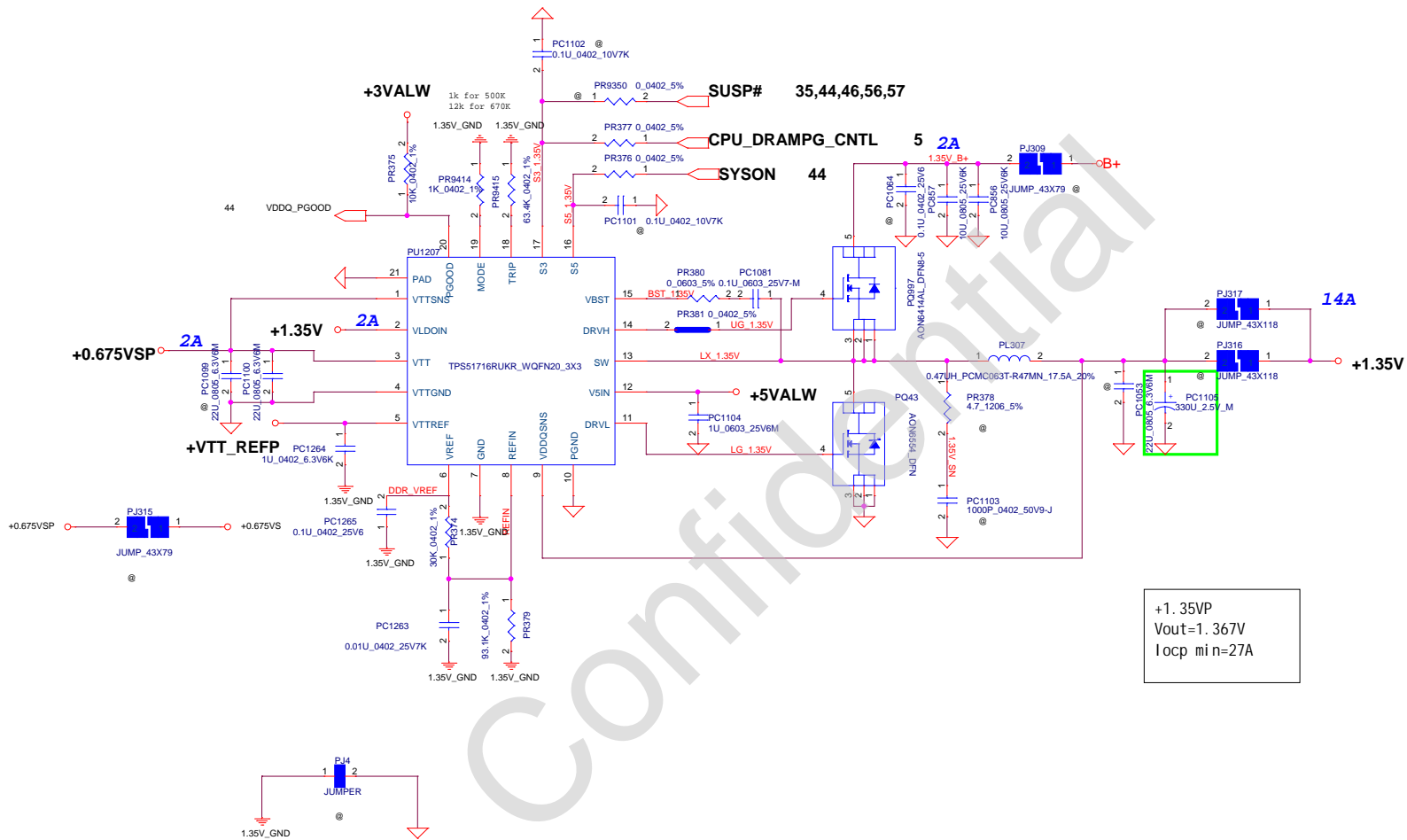
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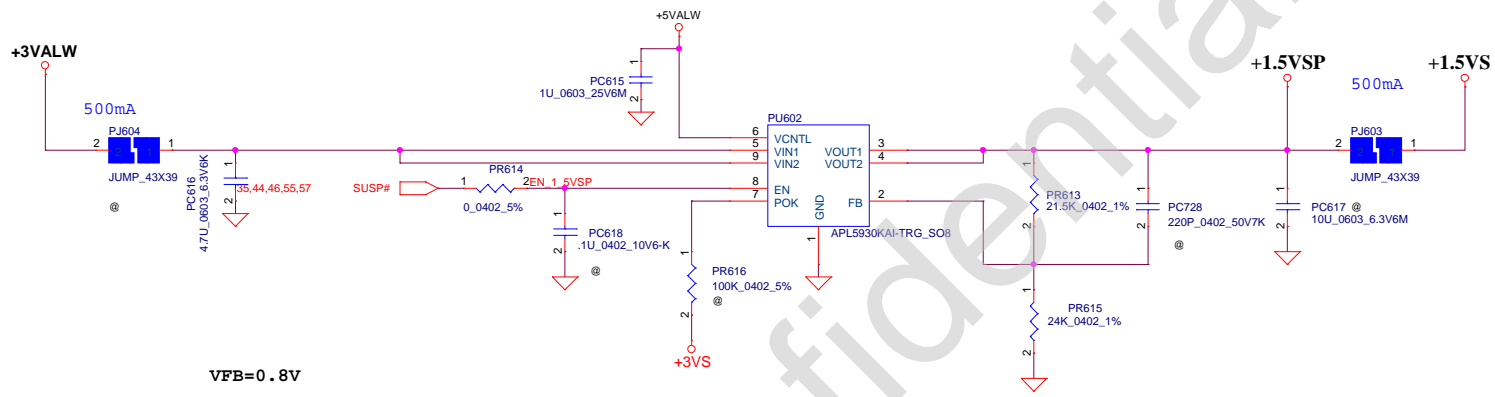


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PWR_3VALW/5VALW		
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1	ACUDA	1.0
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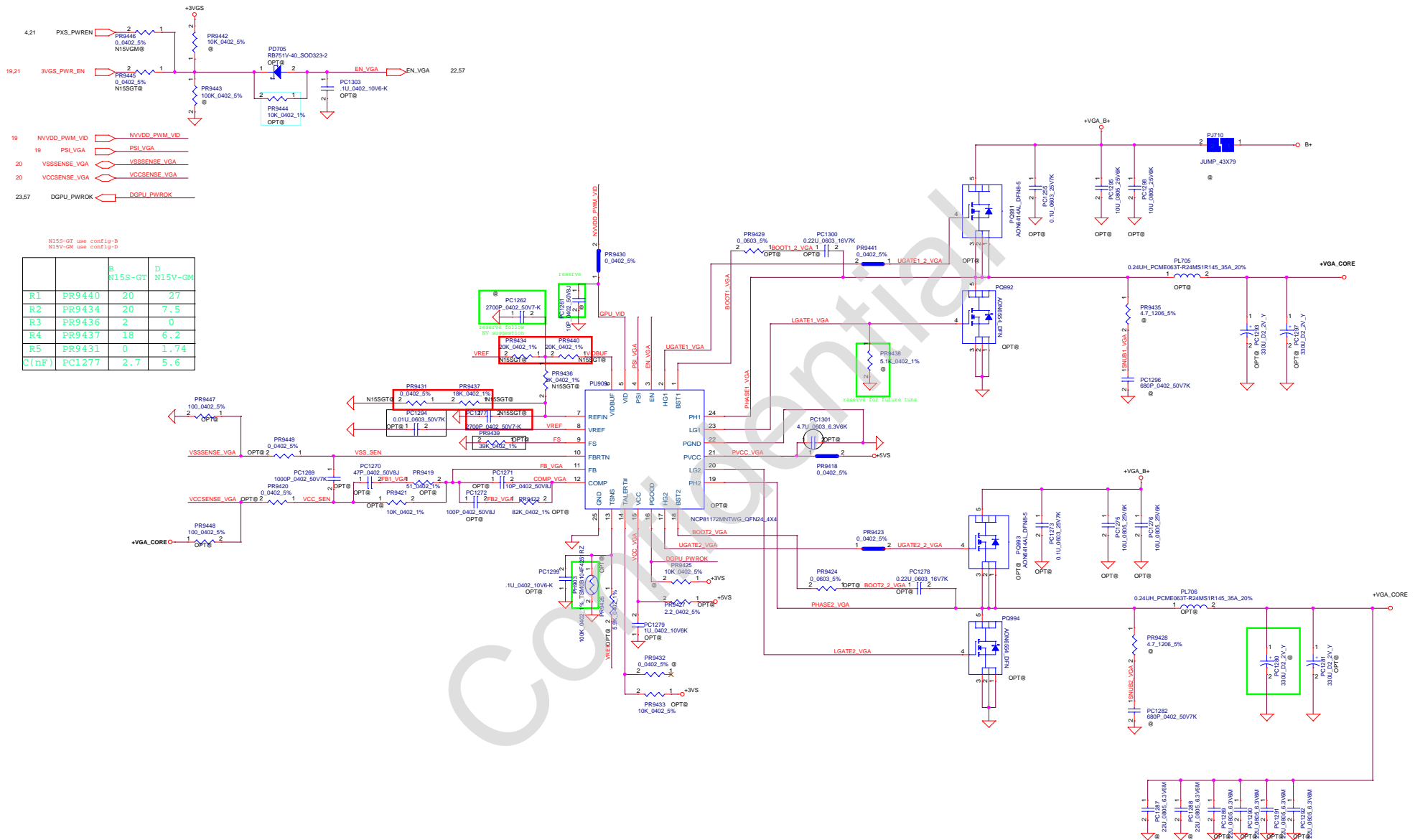


VFB=0.8V

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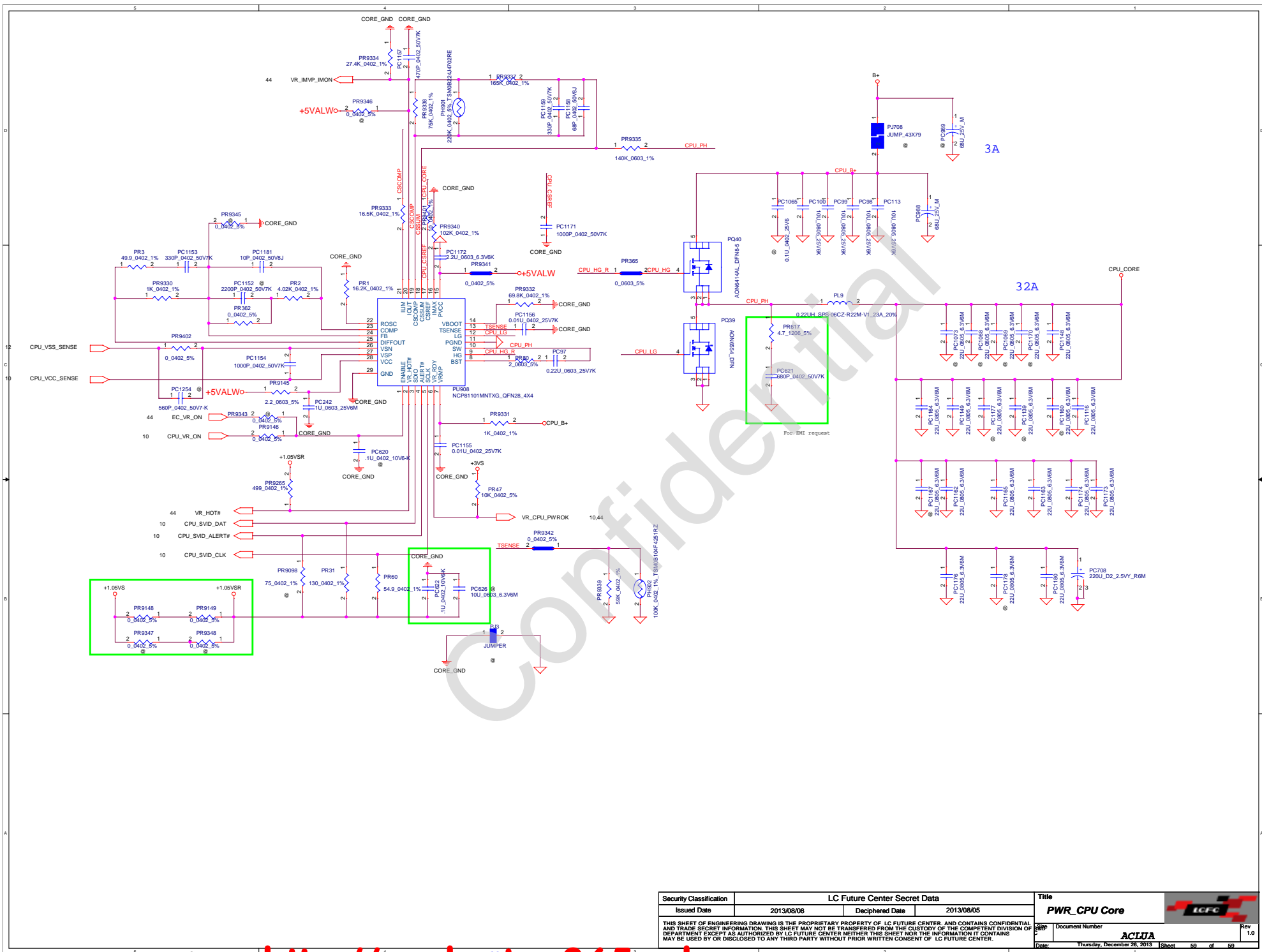
Title		
+1.35VS_VGA/+1.5VS		
Size	Document Number	Rev
Custom	ACLUA	1.0
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N155-GT use config-B
N15V-GM use config-D

	B	D
R1	PR9440	20
R2	PR9434	20
R3	PR9436	2
R4	PR9437	18
R5	PR9431	0
C(nF)	PC1277	2.7

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			PWR-VGA_CORE
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PWR_CPU Core		
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