LCFC NM-C781

GS452/GS552/GS752 MB Schematics Document

CometLake_U42 with DDR4 + Nvidia N16V-GM

2018-01

REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page		
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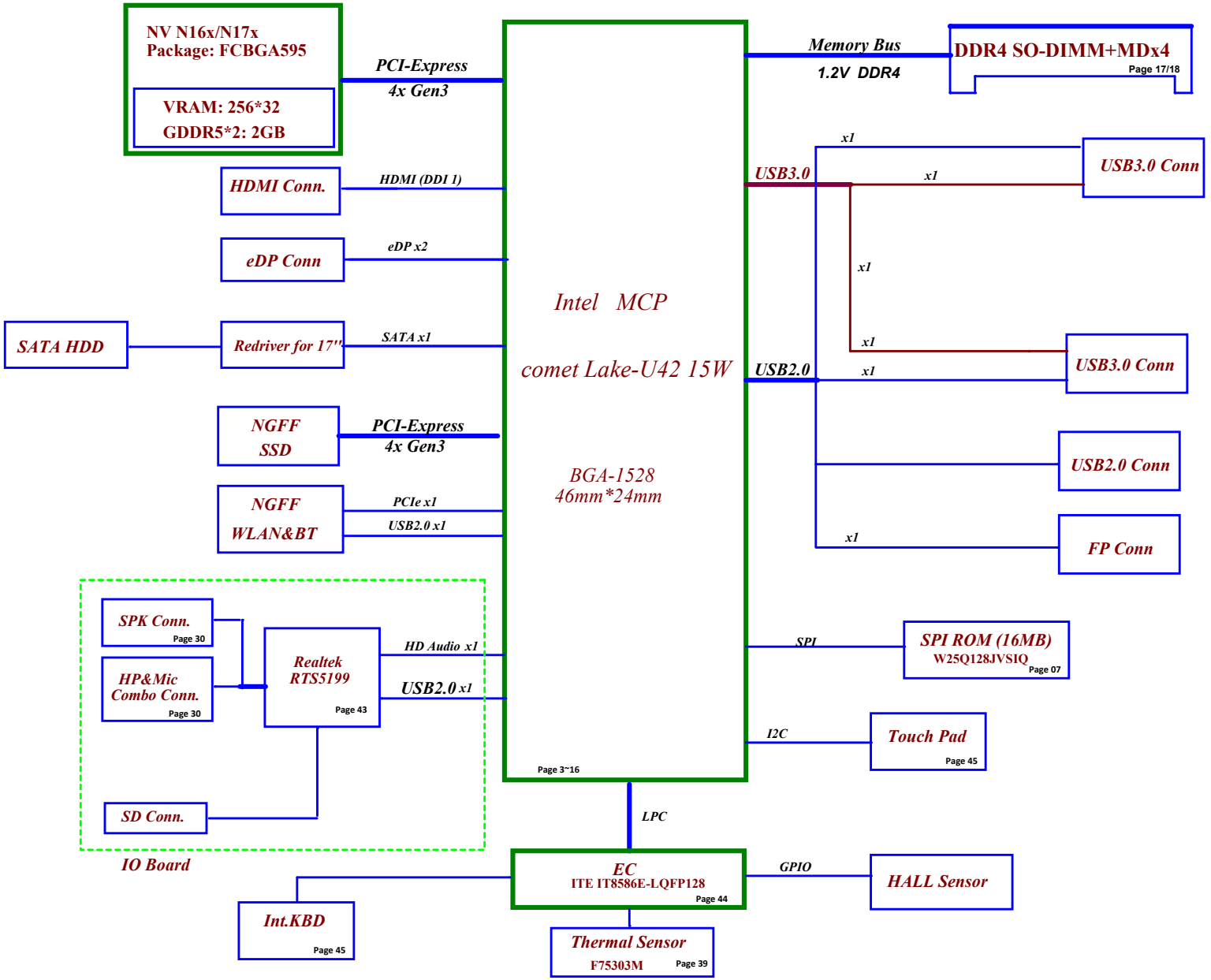

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn
	2	NC
	3	USB3.0 Conn
	4	USB2.0 conn
	5	Card reader
	6	Touch Screen
	7	Camera
	8	NC
	9	NC
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530S part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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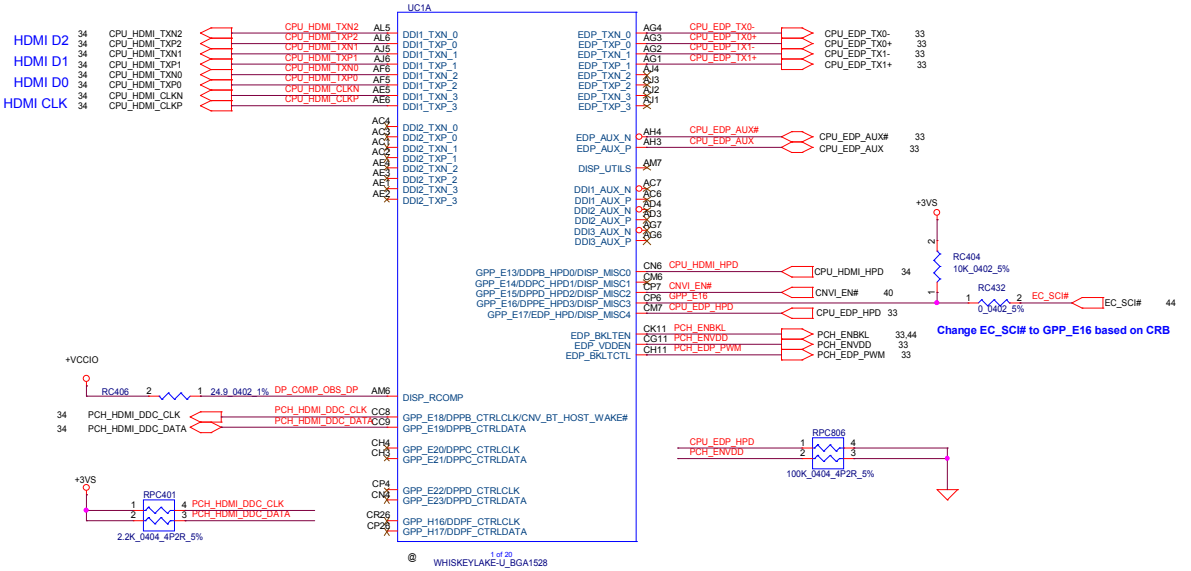
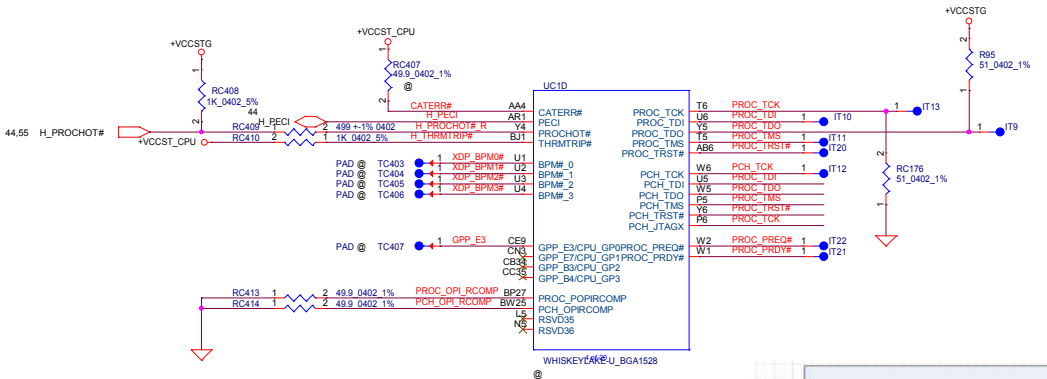
DDP*_CTRLDATA strapping sampled on the rising edge of PCH_PWROK

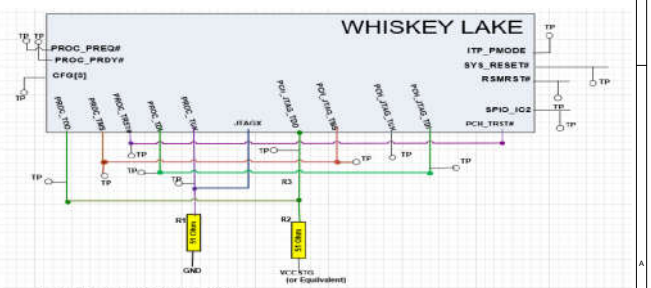
Port	Strap	Enable	Disable
Port 1	GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Pull up to 3.3 V with 2.2Kohm *	NC
Port 2	GPP_E21 / DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Port 3	GPP_E23 / DDPD_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Reserve	GPP_H17/ DPPF_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *

100Ohm for CNL

+VCCIO&EDP_COMP :
Trace Width: 20mil
Isolation Spacing: 25mil
Max length: 100mil







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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (DDI,EDP)**

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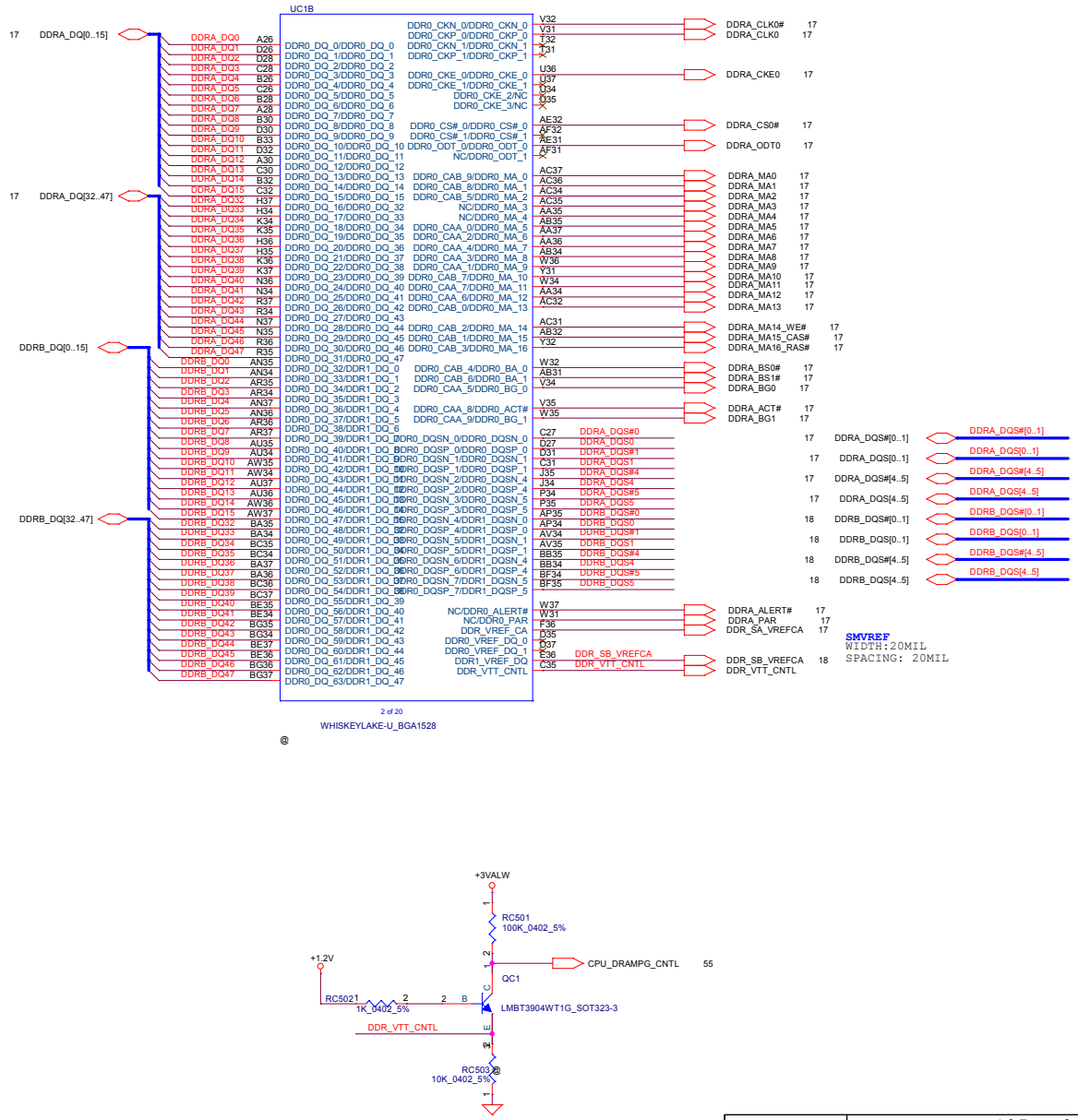

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (DDR4)

Size	Document Number	Rev
Custom	FS441/FS540	0.1
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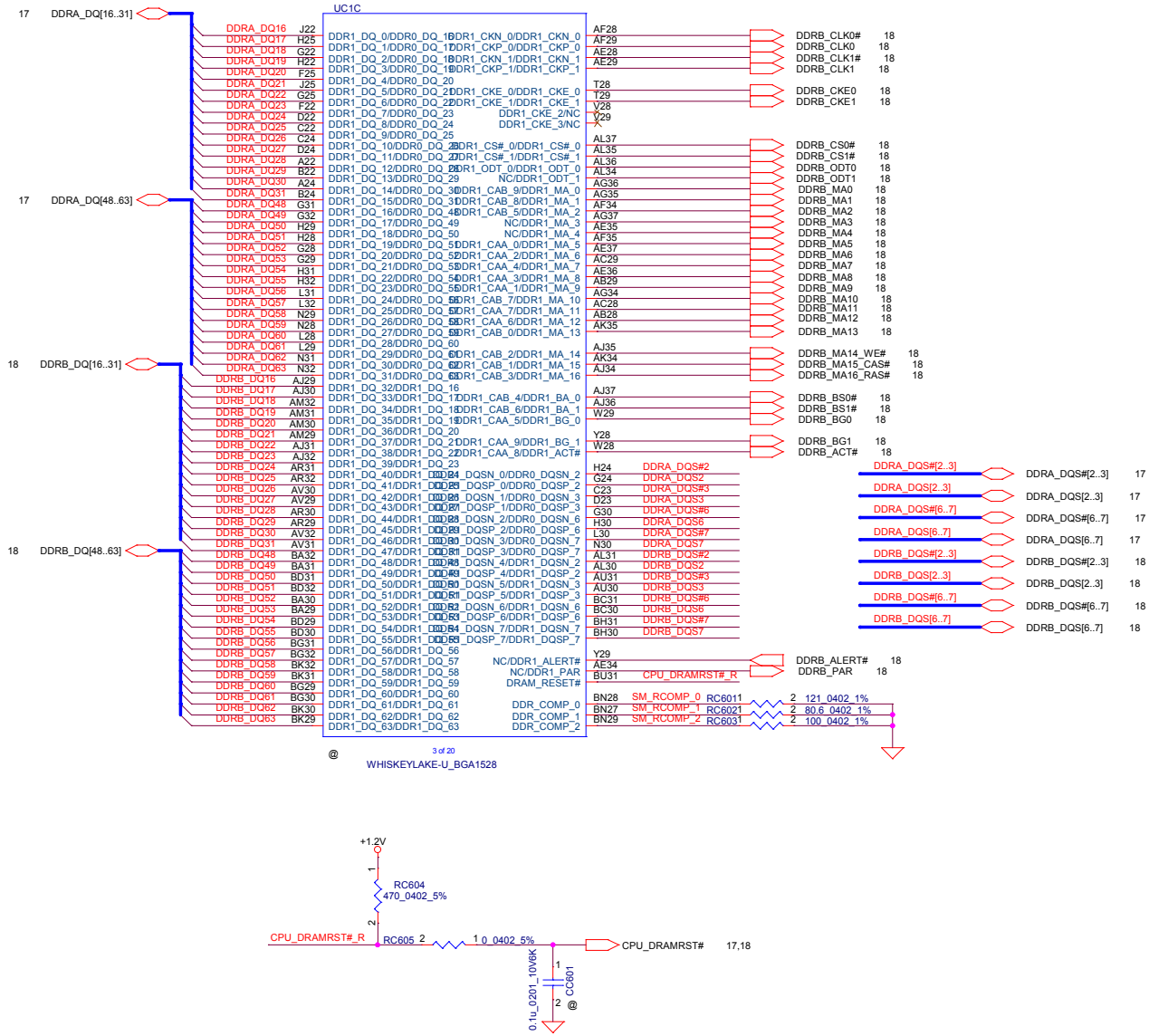

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (DDR4)

Size: Custom	Document Number: FS441/FS540	Rev: 0.1
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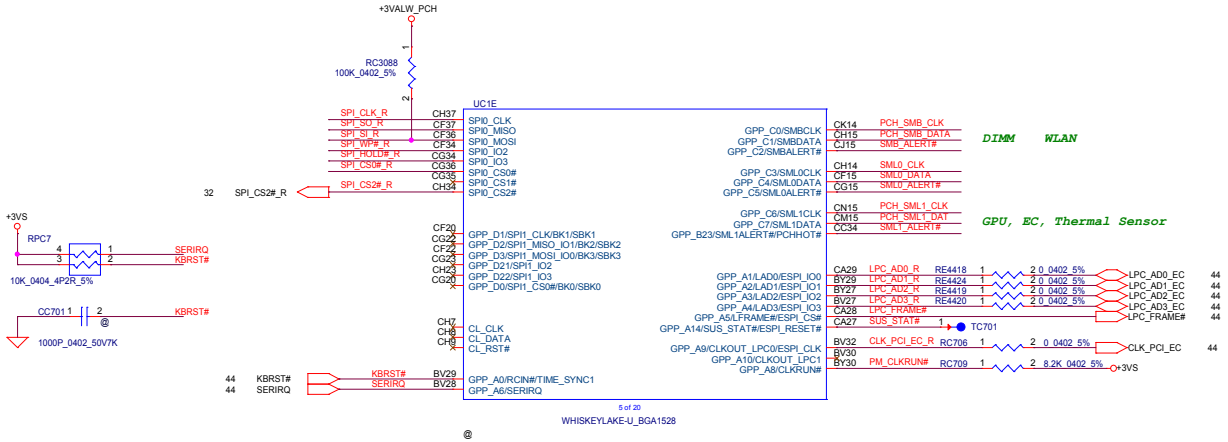
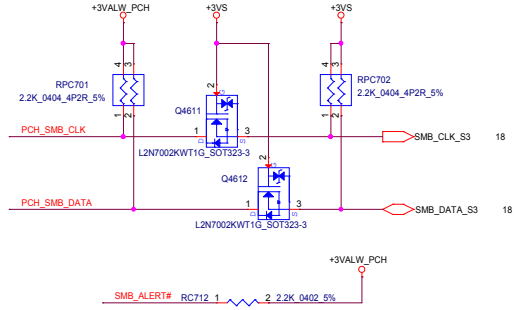
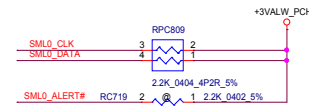


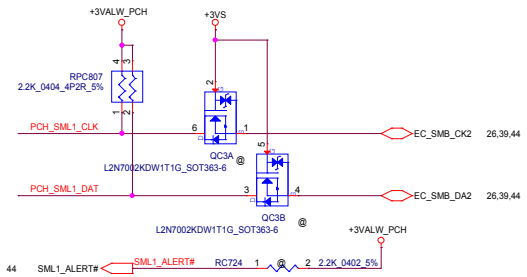
SMBUS&SMLINK



TLS Confidentiality (Rising edge of RSMRST#)
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security(TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

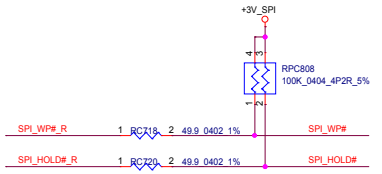


eSPI or LPC (Rising edge of RSMRST#)
This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

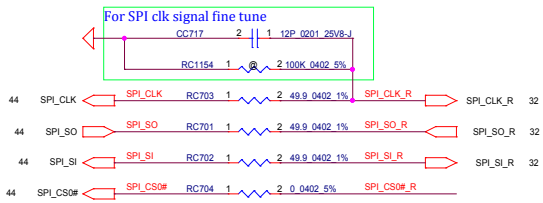


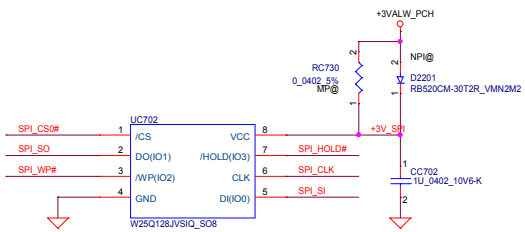
Intel DCI-OOB (Rising edge of RSMRST#)
This signal has an internal pull-down.
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
This signal is in the primary well.

SPI ROM



SPI0_MOSI: Reserved (Rising edge of RSMRST#)
SPI0_IO2: Reserved (Rising edge of RSMRST#)
SPI0_IO3: Reserved (Rising edge of RSMRST#)
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.





LPC R/C close to PCH

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Title	MCP (JTAG,SPI,LPC,SMB)		
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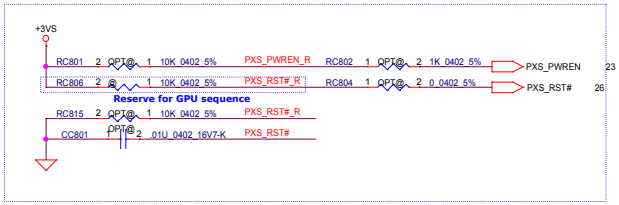
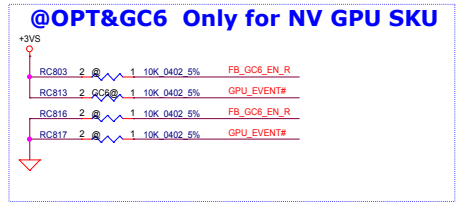
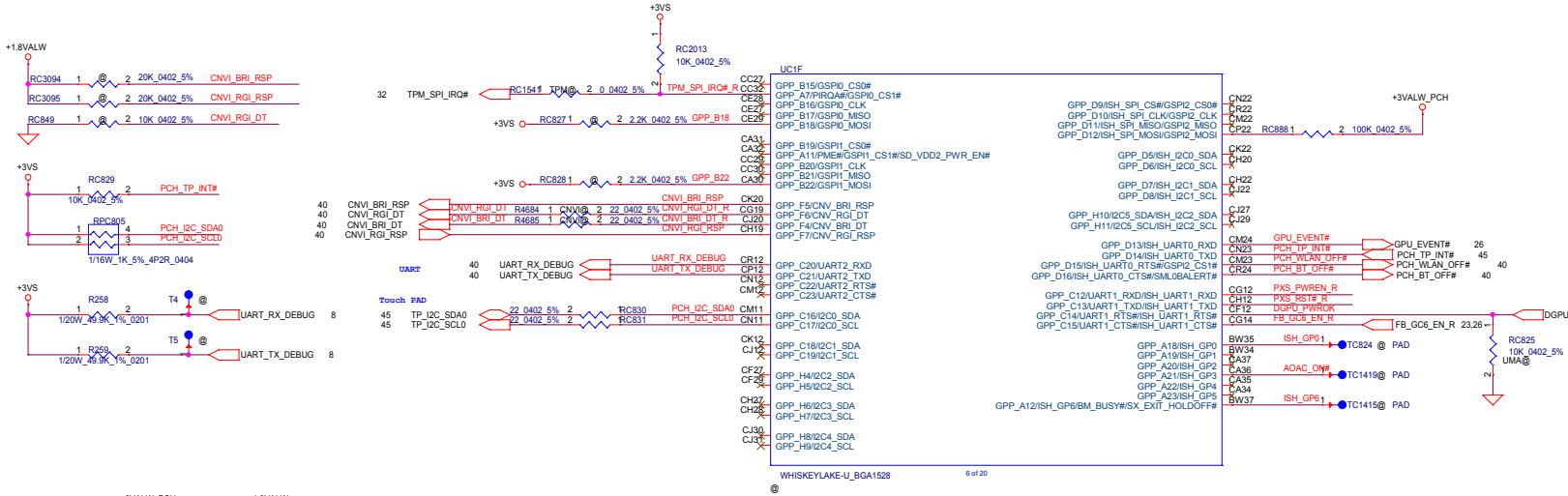
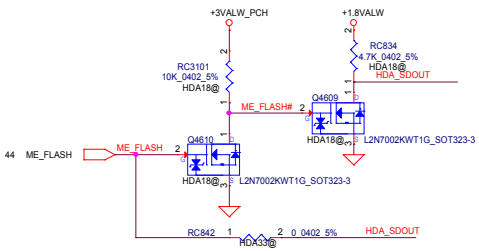
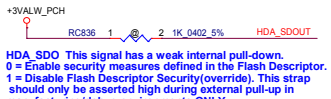


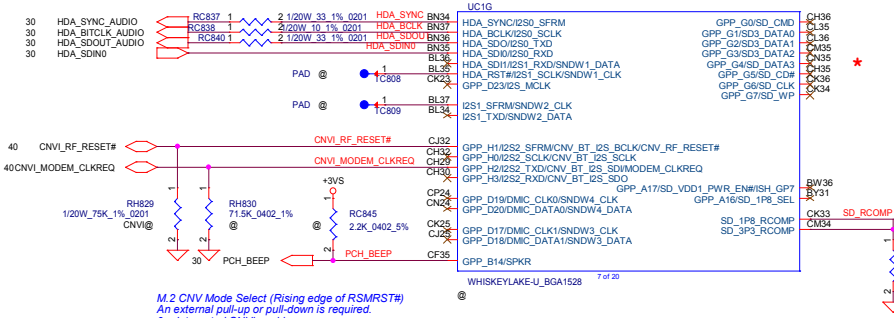








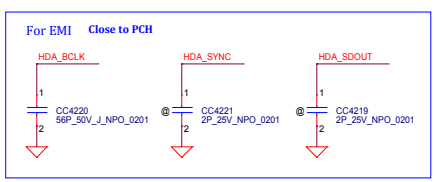
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



M.2 CNV Mode Select (Rising edge of RSMRST#)
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

GPP_B18_NO_REBOOT
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



Note: CNVi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVi is enabled. There must not be any pull-down resistor connected on the board.

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Title: MCP (LPSS,ISH,AUDIO,SDI

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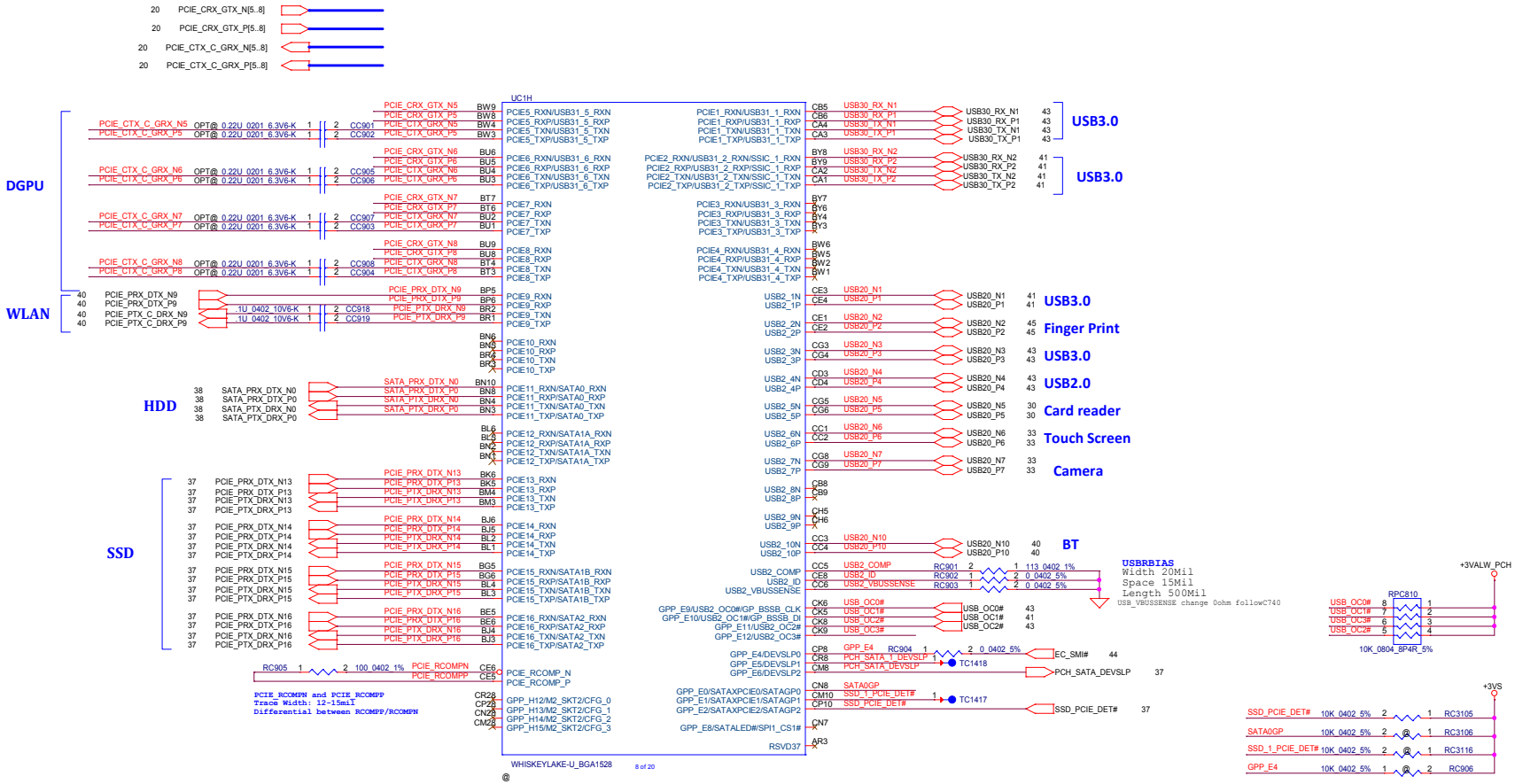

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Title: MCP (PCIE,SATA,USB3.USB

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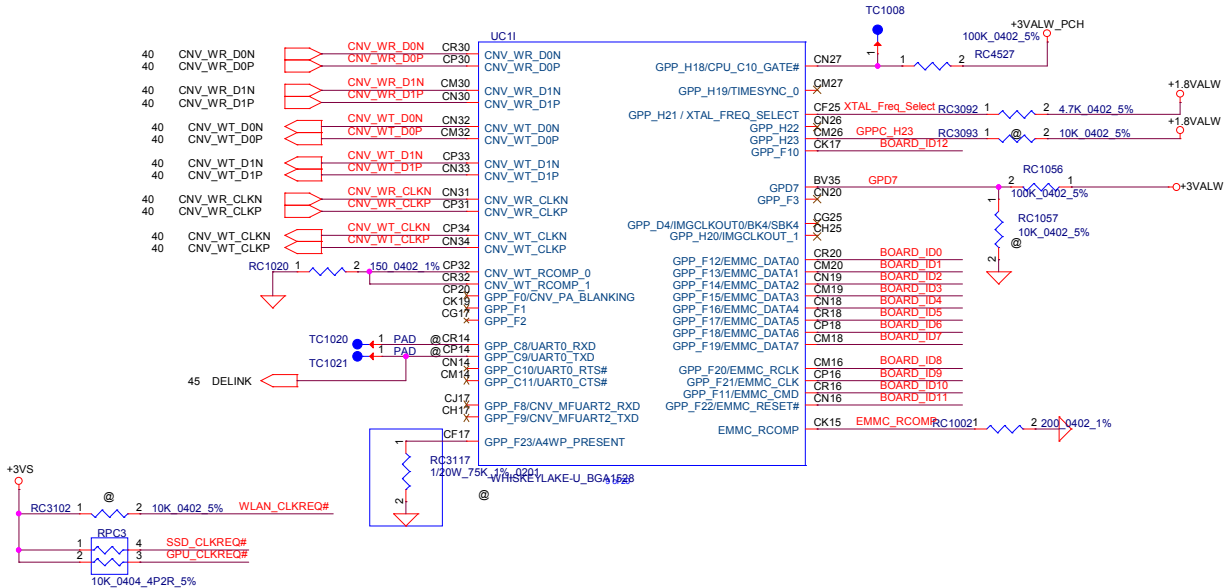
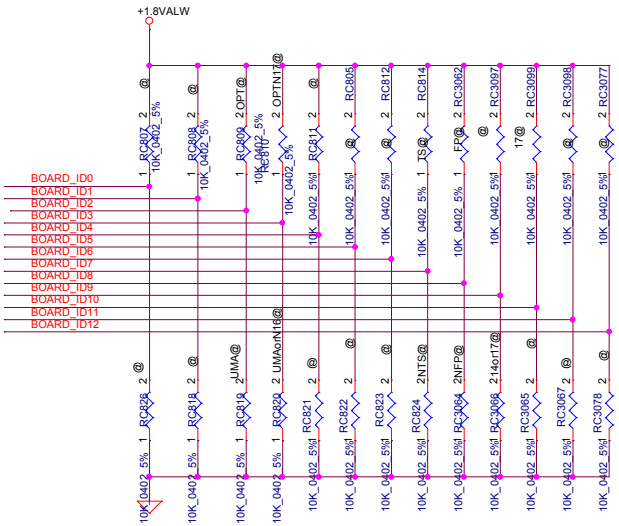
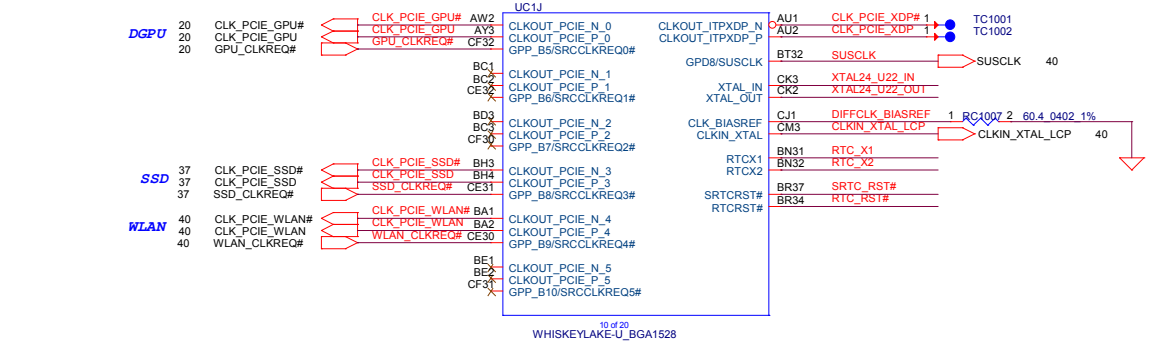
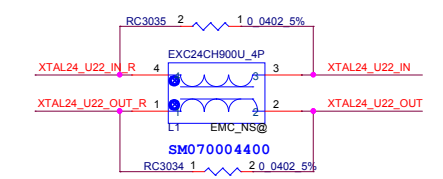
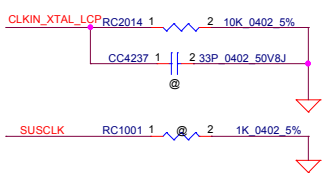
RC3066&RC3065 &RC3097 需要
change bom stucture :common design 14&15;
15@&14or15@------@;14or17@---- KEEP

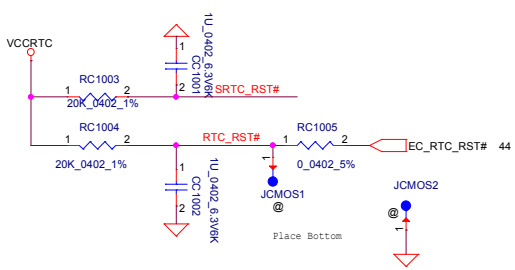


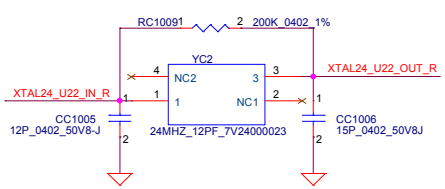


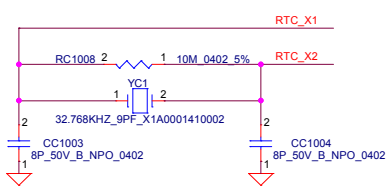












Board ID	Function	Description		Stuff R		
					ID1(GPP_F13)	ID0(GPP_F12)
					PU:RC808	PU:RC807
					PD:RC818	PD:RC826
BOARD ID[1:0]	PROJECT ID(RESERVE)	00				
		01				
		10				
		11				
					ID3(GPP_F15)	ID2(GPP_F14)
					PU:RC810	PU:RC809
					PD:RC820	PD:RC819
Board ID[3:2]	GPU ID	00	UMA		0 (RC820)	0 (RC819)
		01	DIS+N16x		0 (RC820)	1 (RC809)
		10				
		11	DIS+N17x		1 (RC810)	1 (RC809)
				ID6(GPP_F16)	ID5(GPP_F17)	ID4(GPP_F16)
				PU:RC812	PU:RC805	PU:RC811
				PD:RC823	PD:RC822	PD:RC821
Board ID[6:4]	Memory Down ID	000	SAM4G			
		001	SAM8G	0 (RC823)	0 (RC822)	1 (RC811)
		010	MICRON4G			
		011	MICRON8G	0 (RC823)	1 (RC805)	1 (RC811)
		100	HY4G			
		101	HY8G	1 (RC812)	0 (RC822)	1 (RC811)
		110				
		111	SODIM(NO on board)	1 (RC812)	1 (RC805)	1 (RC811)
						ID7(GPP_F19)
						PU:RC814
						PD:RC824
Board ID7	Touch SCREEN ID	0	NTS			0 (RC824)
		1	TS			1 (RC814)
						ID8(GPP_F20)
						PU:RC3062
						PD:RC3064
Board ID8	FP ID	0	NFP			0 (RC3064)
		1	FP			1 (RC3062)
					ID10(GPP_F11)	ID9(GPP_F21)
					PU:RC3099	PU:RC3097
					PD:RC3065	PD:RC3066
Board ID[10:9]	Panel Size	00	14"		0 (RC3065)	0 (RC3066)
		01	15"		0 (RC3065)	1 (RC3097)
		10	17"		1 (RC3099)	0 (RC3065)
		11	Reserved			
						ID11(GPP_F22)
						PU:RC3098
						PD:RC3067
Board ID11	RESERVE					
						ID12(GPP_F10)
						PU:RC3077
						PD:RC3078
Board ID12	RESERVE					

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Title: MCP (CSI2,EMMC,CLOCK)

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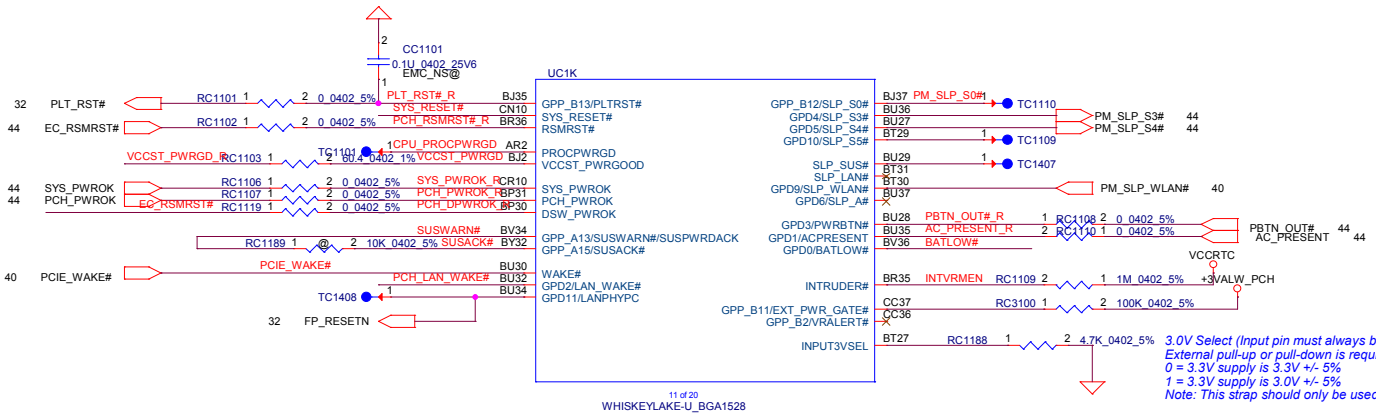
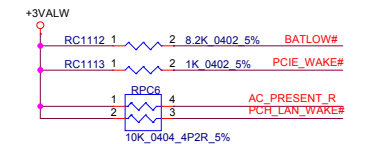
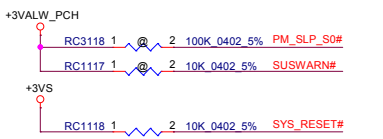
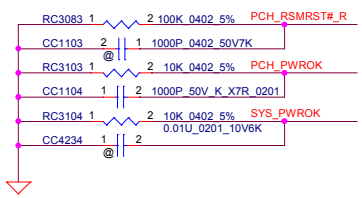
- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

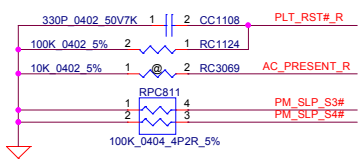


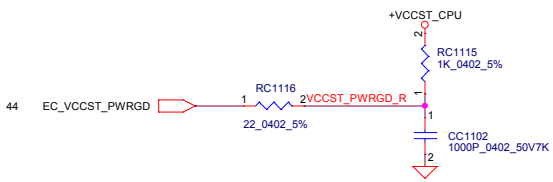
3.0V Select (Input pin must always be driven to a valid logic level)
External pull-up or pull-down is required
0 = 3.3V supply is 3.3V +/- 5%
1 = 3.3V supply is 3.0V +/- 5%
Note: This strap should only be used for specific targeted 1S battery systems

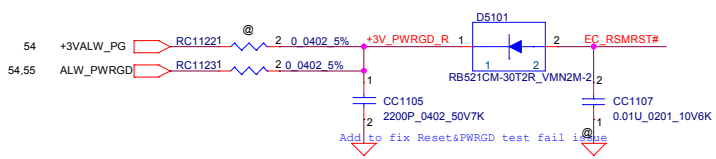


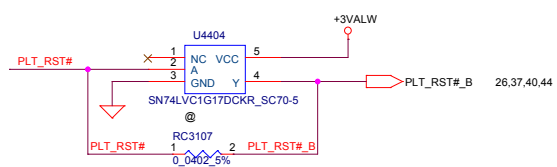


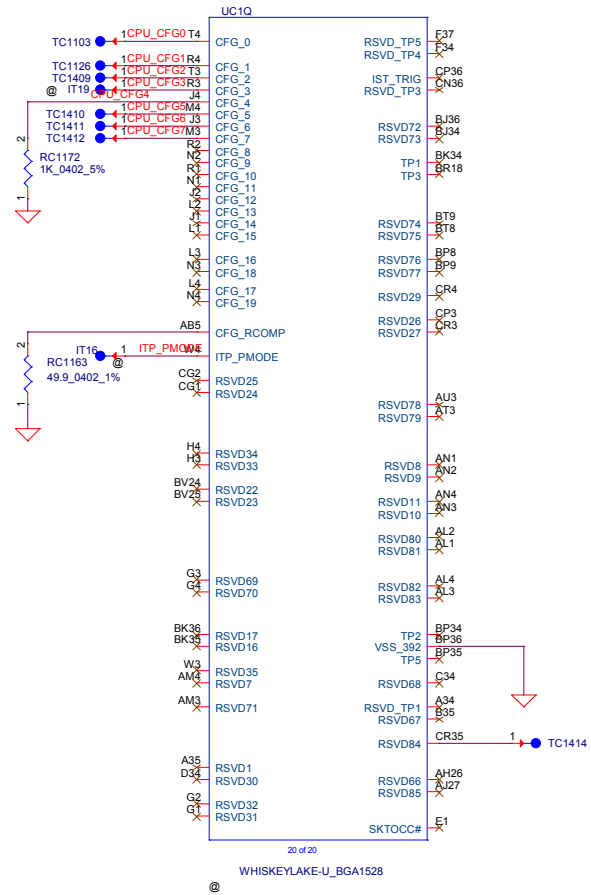








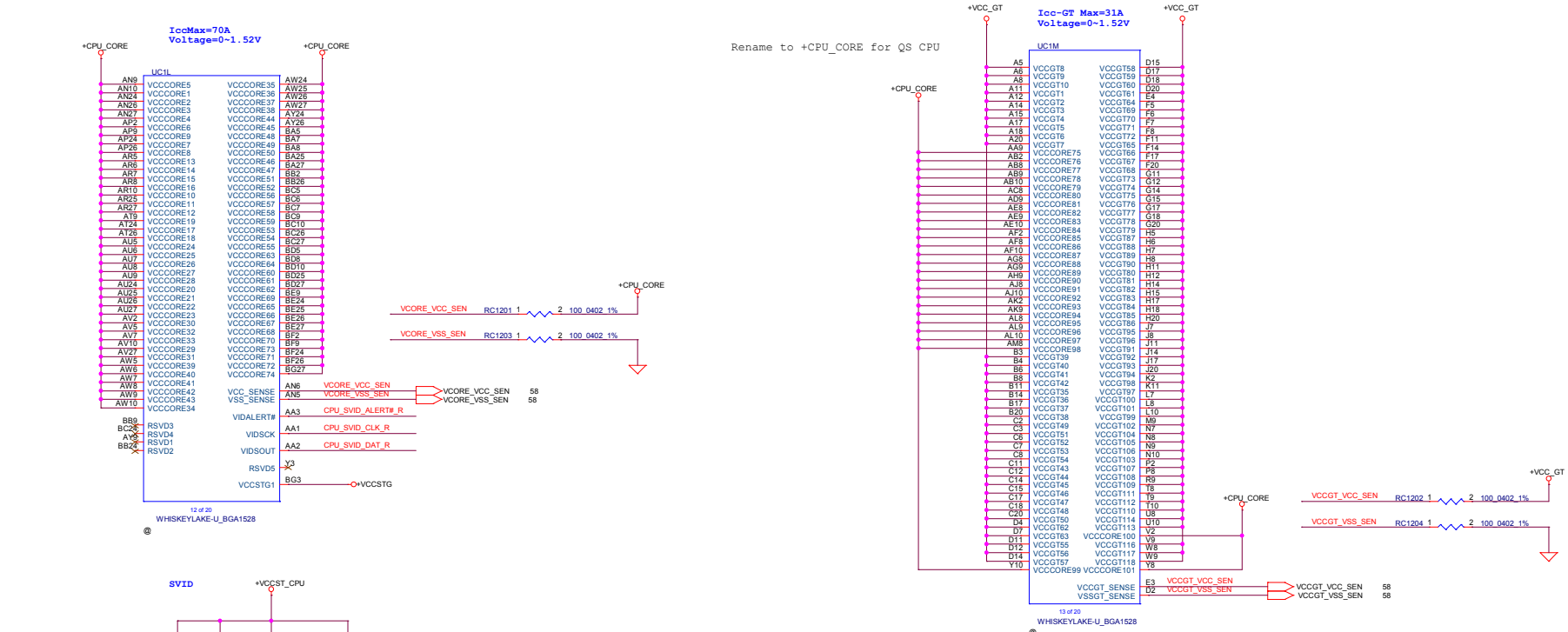




Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (SYSTEM PWR MANAGEMENT)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1
Date: Wednesday, October 16, 2019	Sheet 11 of 61	

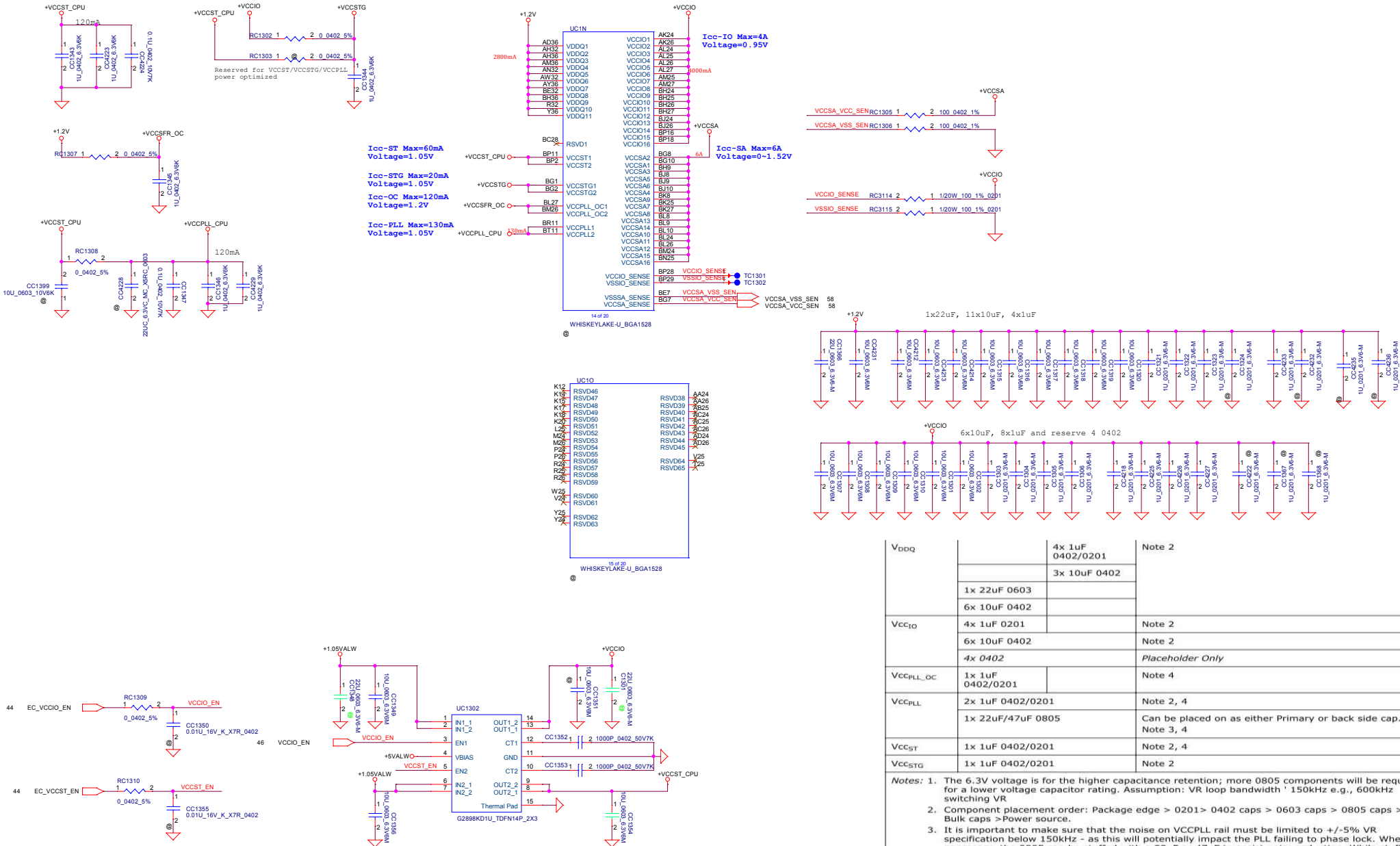


Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: MCP (CPU PWR1)

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

Date: Wednesday, October 16, 2019 | Sheet 12 of 61



V_{DDQ}		4x 1uF 0402/0201	Note 2
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Note 2
	6x 10uF 0402		Note 2
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402/0201		Note 4
Vcc_{PLL}	2x 1uF 0402/0201		Note 2, 4
	1x 22uF/47uF 0805		Can be placed on as either Primary or back side cap. Note 3, 4
Vcc_{ST}	1x 1uF 0402/0201		Note 2, 4
Vcc_{STG}	1x 1uF 0402/0201		Note 2

Notes:

1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 150kHz e.g., 600kHz switching VR
2. Component placement order: Package edge > 0201> 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.
3. It is important to make sure that the noise on VCCPLL rail must be limited to +/-5% VR specification below 150kHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route VCCPLL rail carefully (avoid noisy and high current rail) to mitigate any potential issue.
4. Do not merge VccPLL, VccPLL_OC, VccST to any noisy and high current power rail and do not route them close/adjacent to and reference to any noise and hight current rail on top and bottom layers - as this may impact to PLL failing to phase lock.

Title	MCP (CPU PWR2)	
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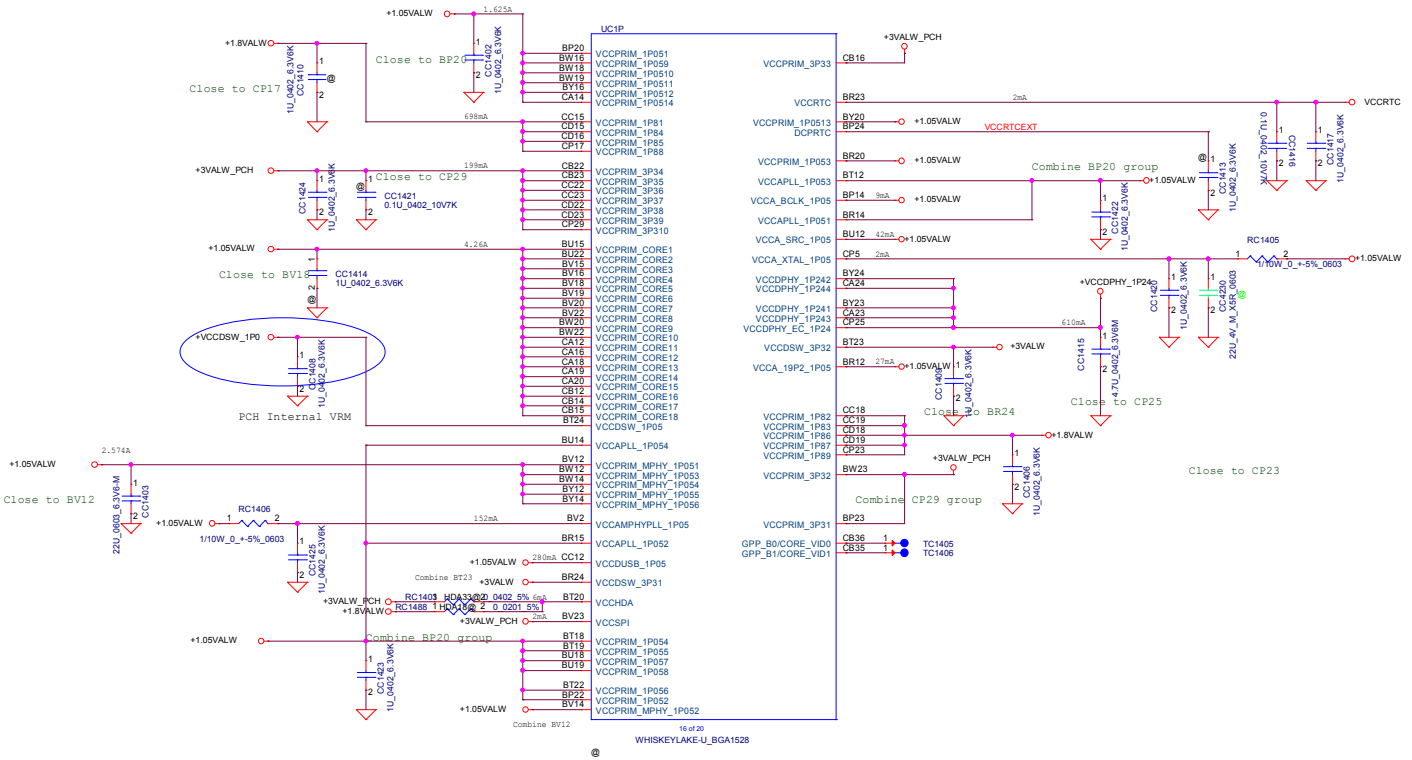
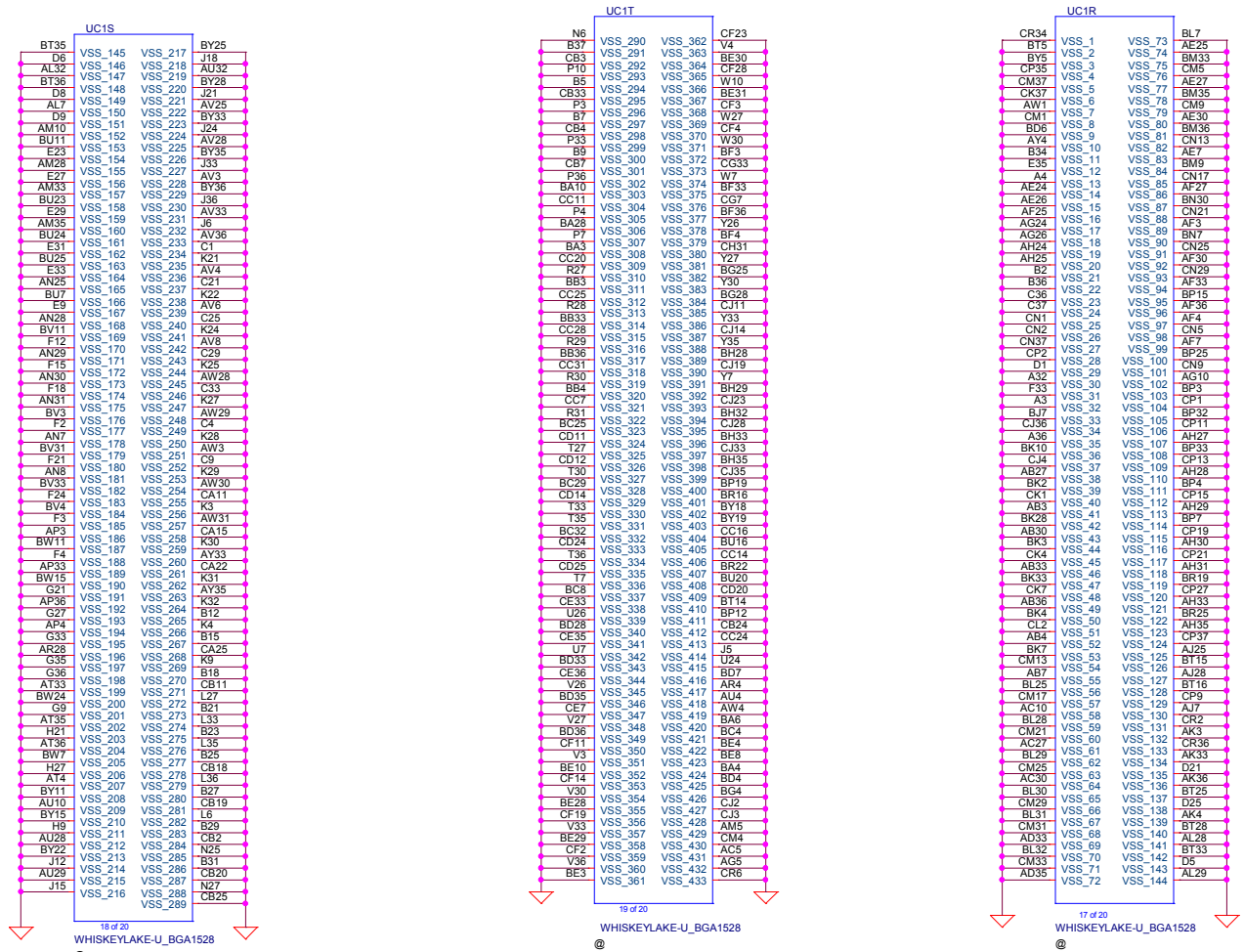
Refer to DOC# 566439-P58



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (PCH PWR)**

Size: Custom	Document Number: **FS441/FS540**	Rev: 0.1
Date: Wednesday, October 16, 2019	Sheet 14 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (VSS)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

Date: Wednesday, October 16, 2019 | Sheet 15 of 61

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: XDP

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

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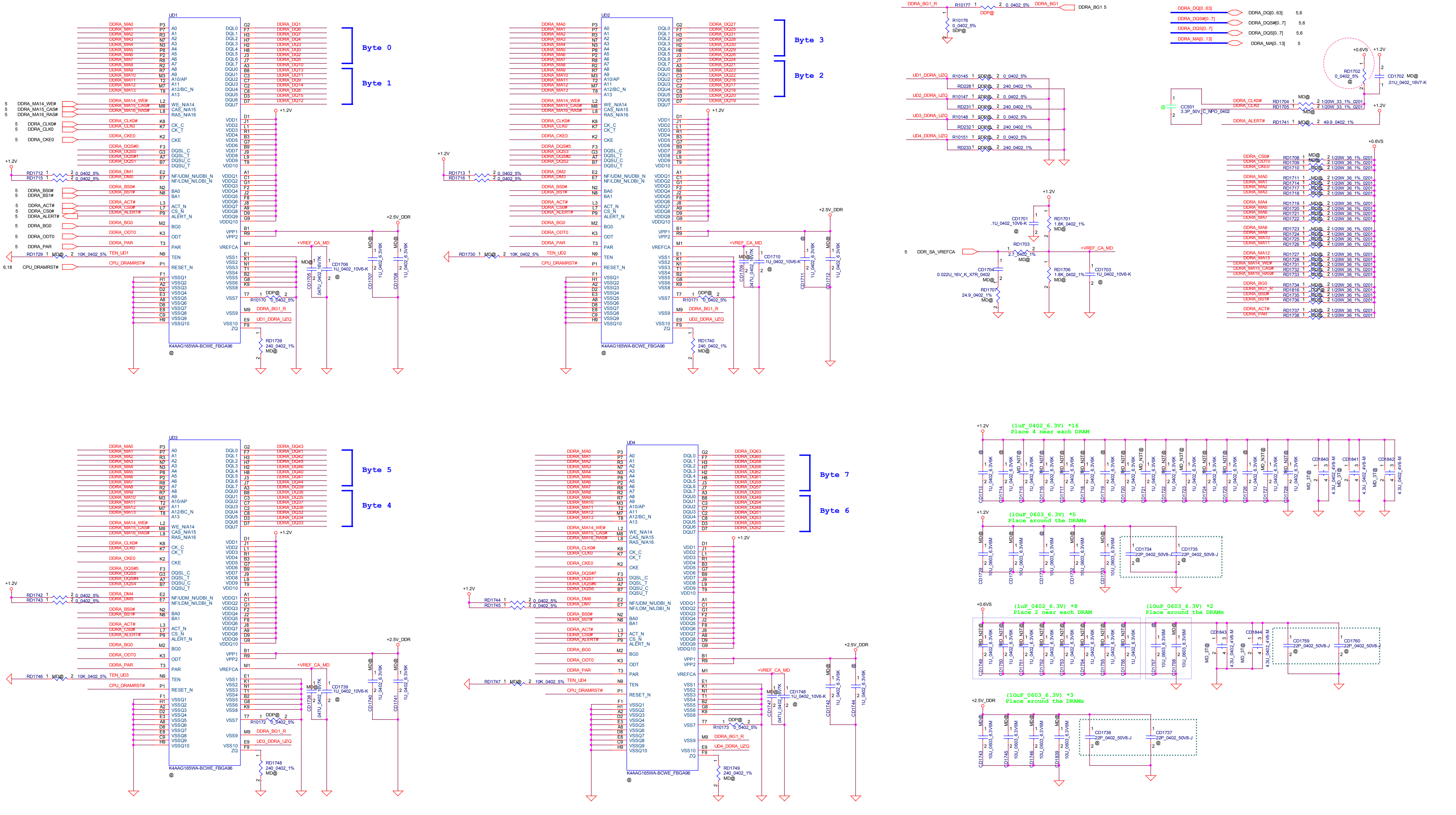
Apply X76 BOM to control DDP Memory Down stuff components!



Security Classification	LC Future Center Secret Data		
Issued Date	2017/06/24	Deciphered Date	2018/06/23

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Title	DDR4 Memory Down		
Custom	Document Number	FS441/FS540	Rev 0.1
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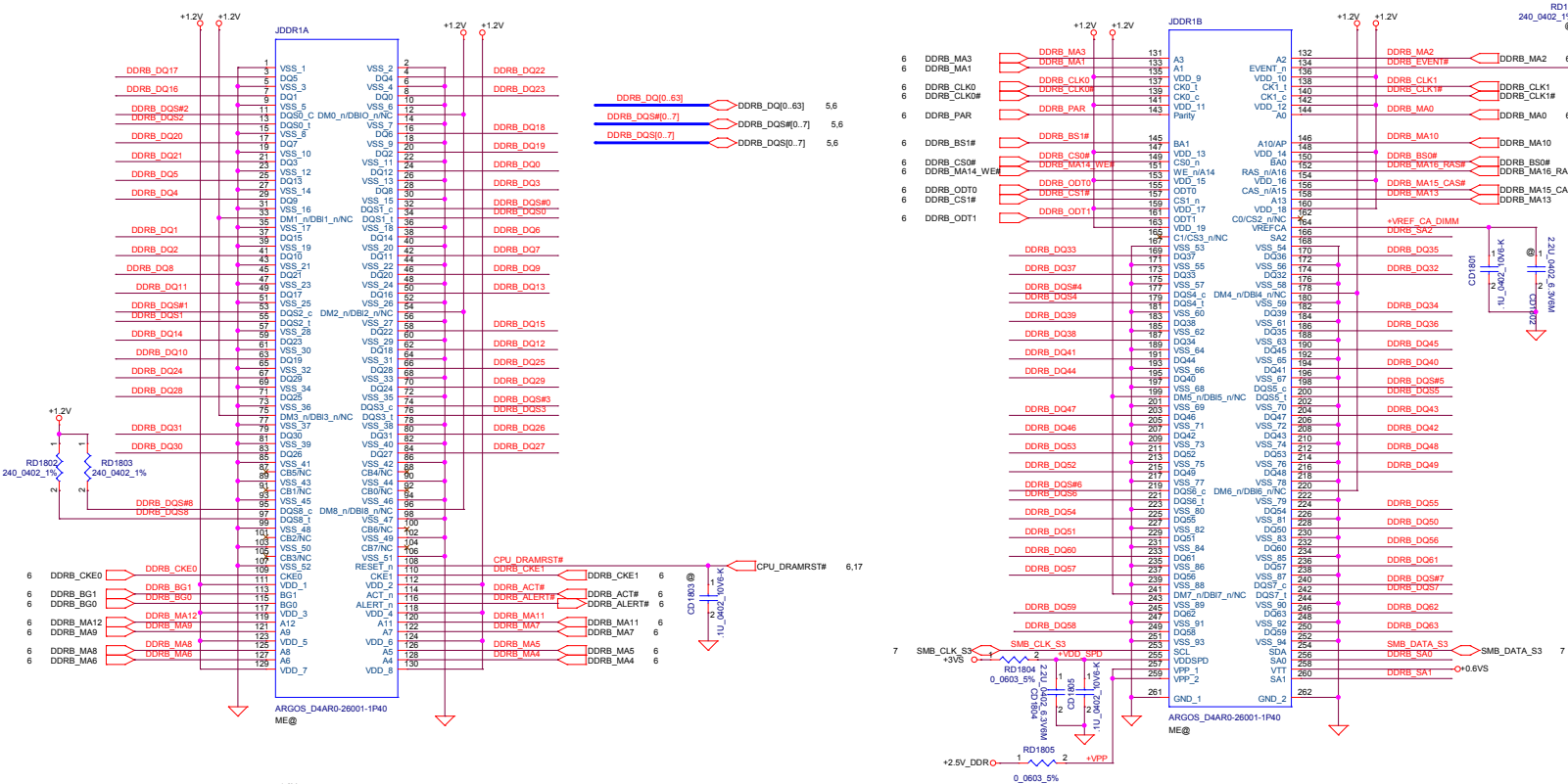
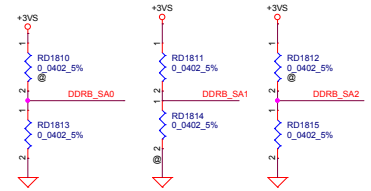
DDR4 SO-DIMM



Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM

SPD address setting



SPD Address = 010

For EMC

Near JDDRL1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: DDR4 SO-DIMM

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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

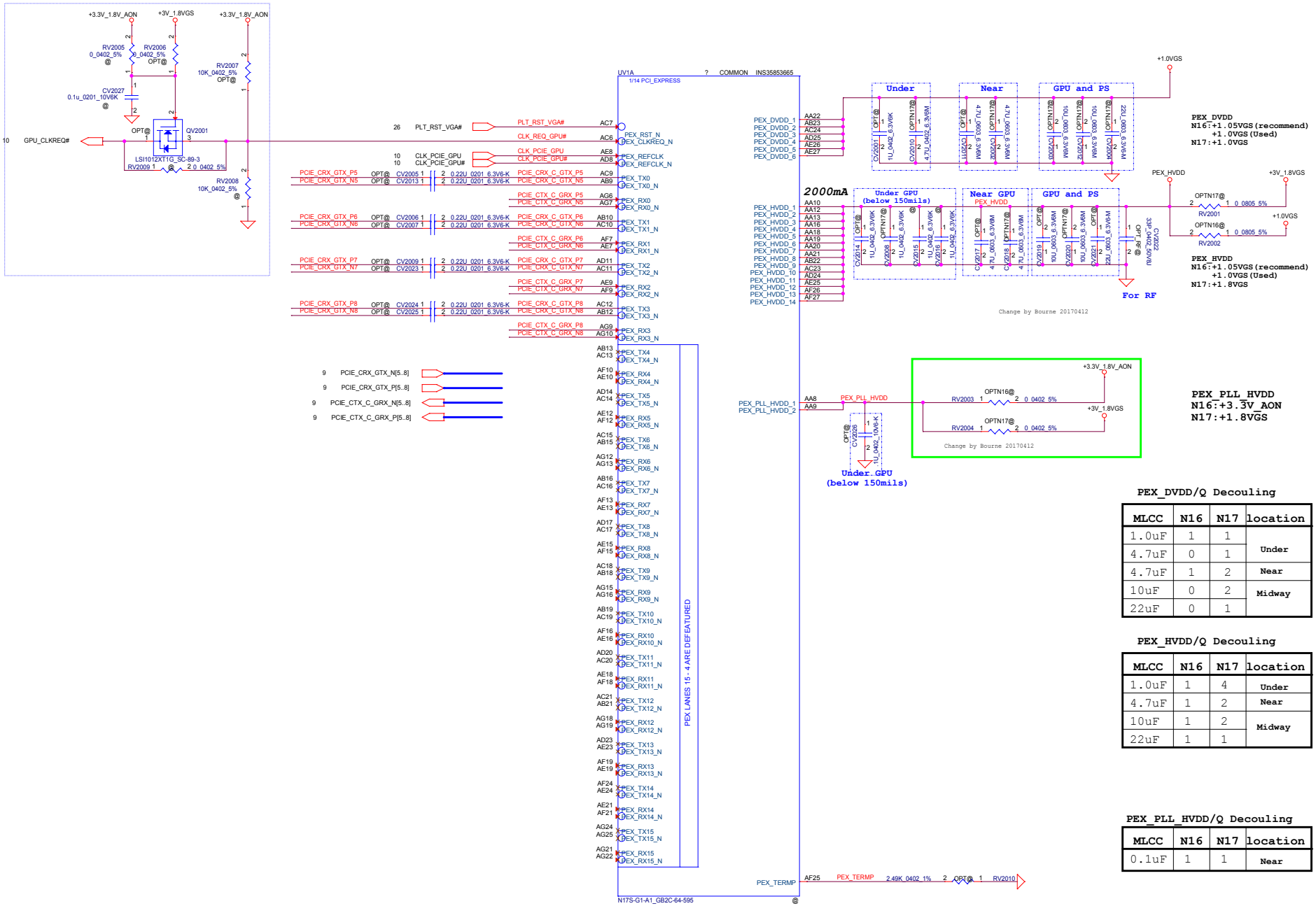
Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	(1.05V) (6) (mA)	(1.05V) (6) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Title: VGA Notes List

Size	Document Number	Rev
C	FS441/FS540	0.1



PEX_PLL_HVDD
N16:+3.3V_AON
N17:+1.8VGS

PEX_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

Title: **GPU_PCIE Interface**

Size	Document Number	Rev
C	FS441/FS540	0.1

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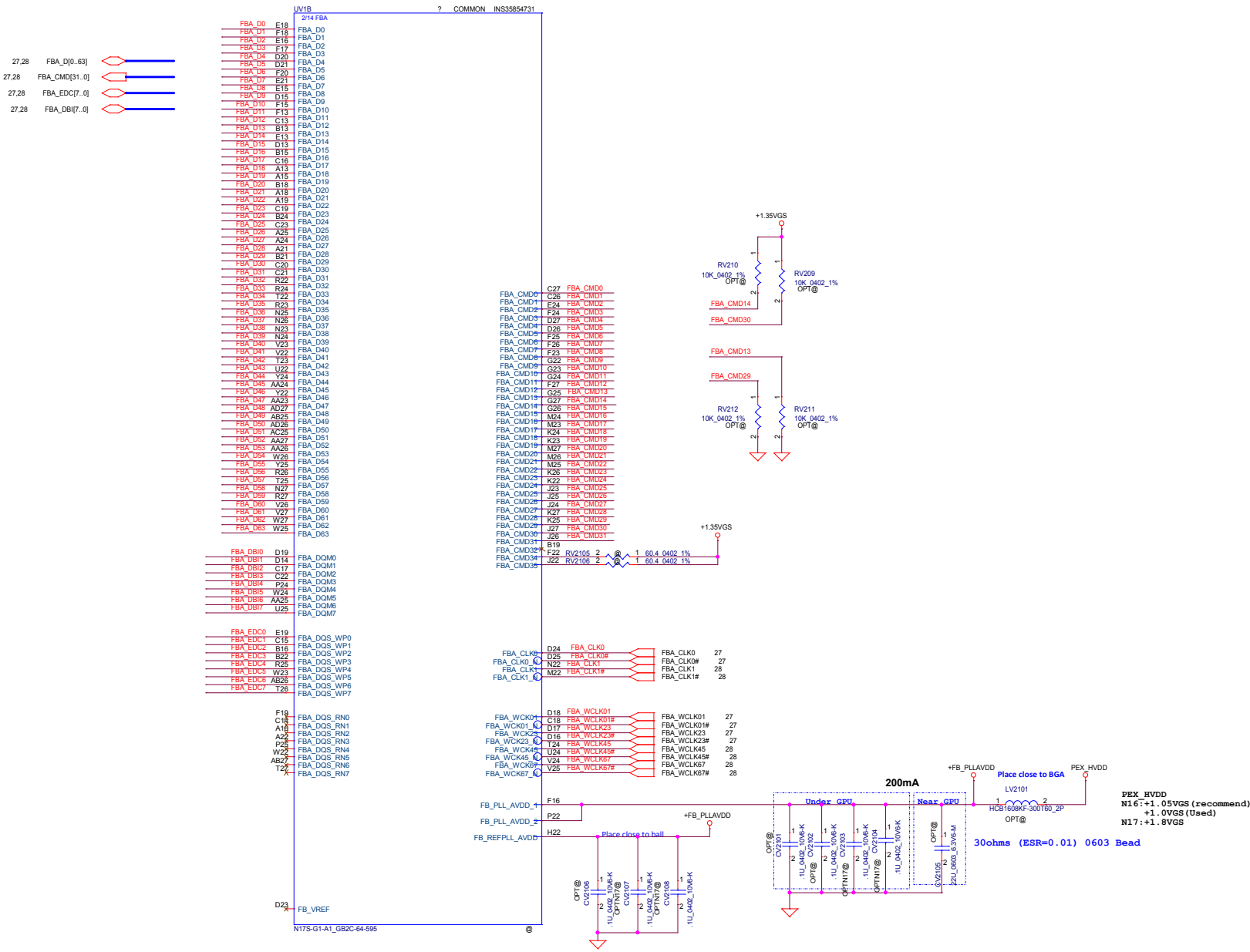

FB_PLL/Q Decouling

MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_MEM Interface**

Size	Document Number	Rev
C	FS441/FS540	0.1

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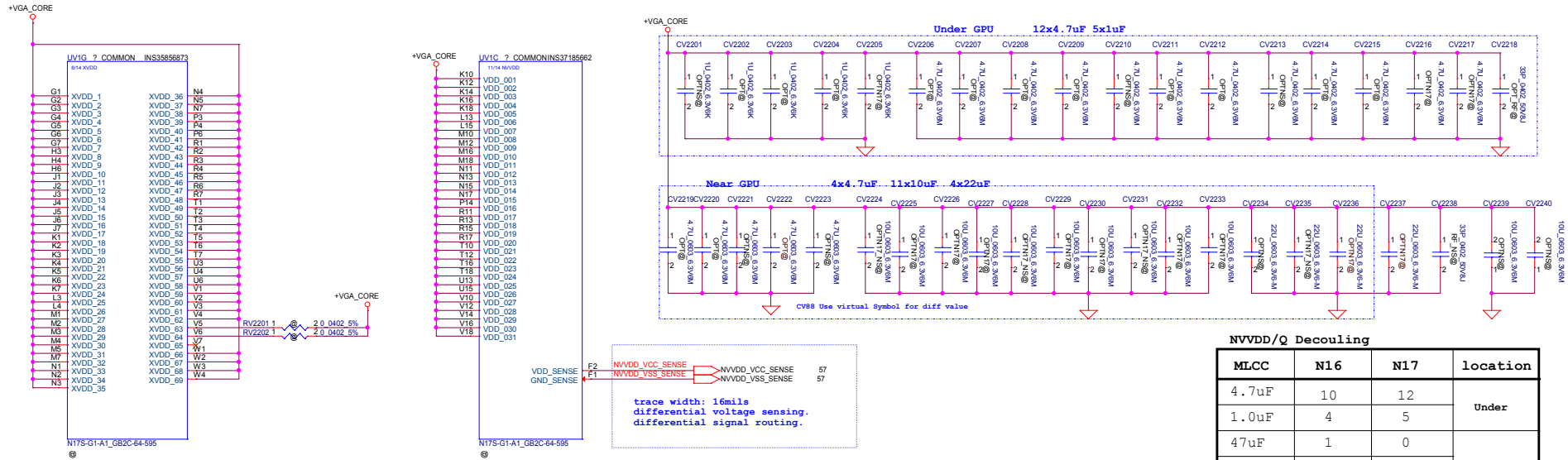
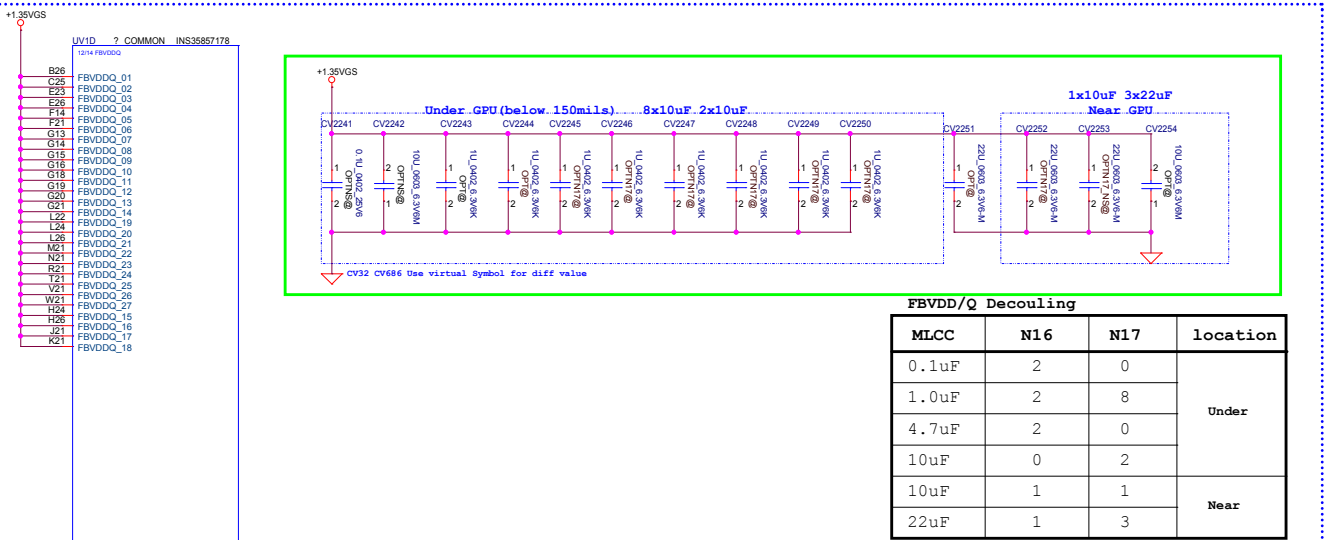


NVVDD/Q Decouling

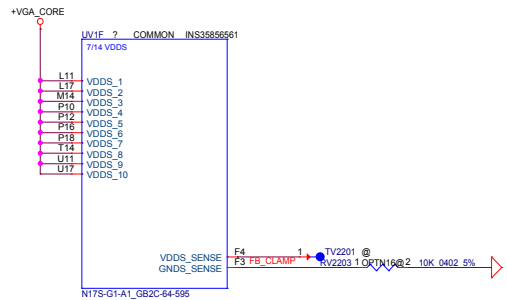
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_+VGA_CORE,FBVDDQ

Size	Document Number	Rev
C	FS441/FS540	0.1

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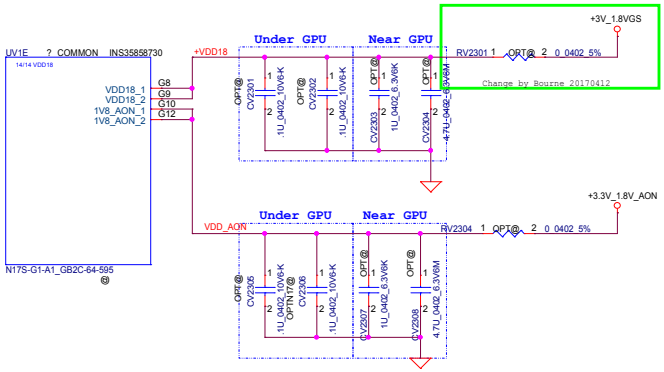
N16 3V3_MAIN(N17 VDD_18) Decouling

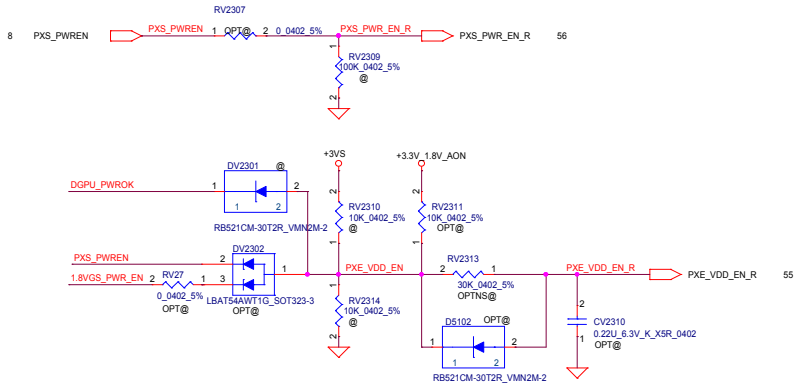
MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

N16 3V3_AON(N17 1V8_AON) Decouling

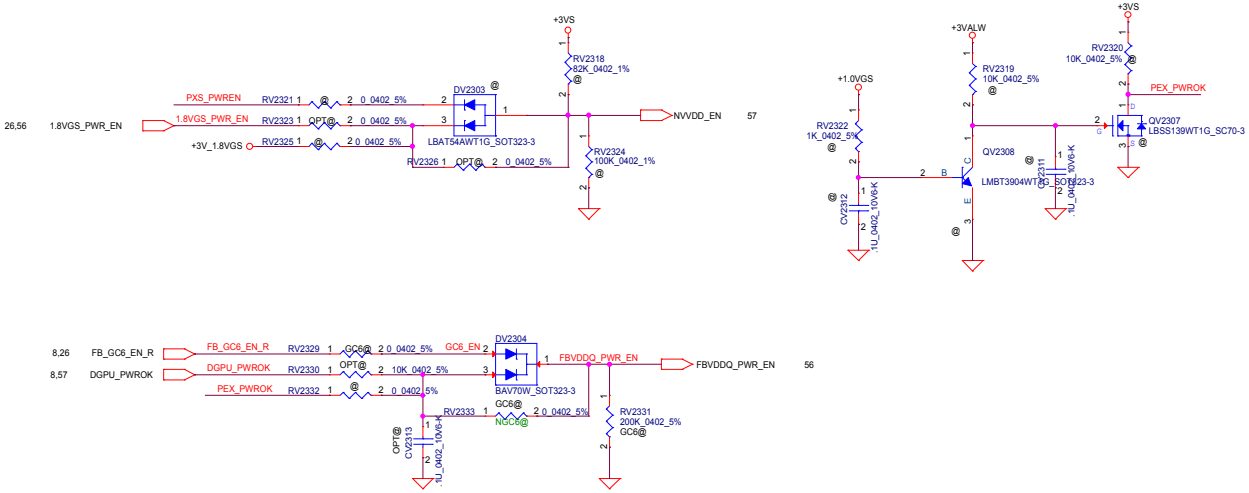
MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	



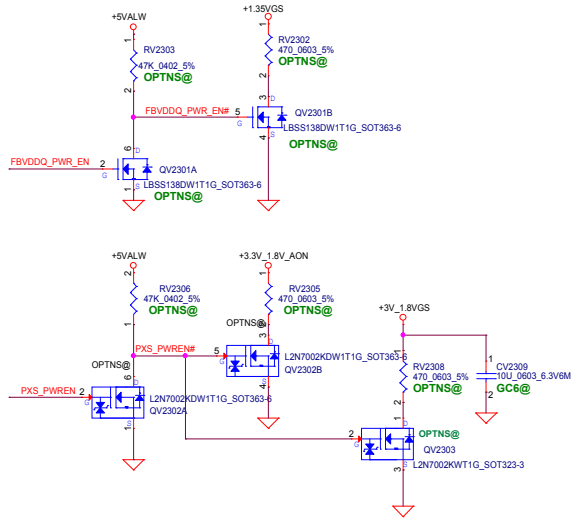
PXE_VDD & 1V8_AON



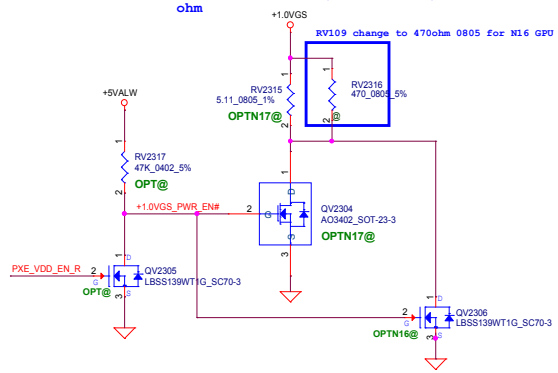
+1.8VG_AON TO +1.8VGS

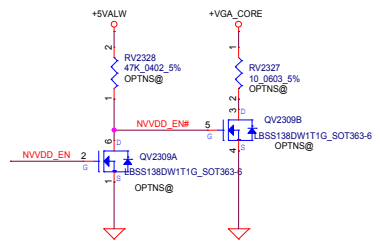


Discharge



RV2316 建虚拟料号,N16=470 ohm,N17=5.11 ohm





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_AON/MAIN PWR/SEQ

Size	Document Number	Rev
C	FS441/FS540	0.1

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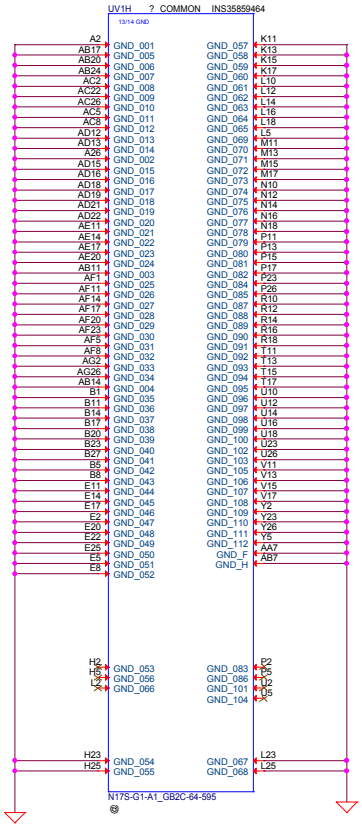

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_GND

Size	Document Number	Rev
C	FS441/FS540	0.1

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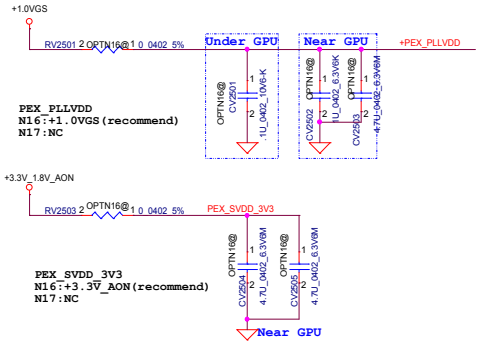
PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

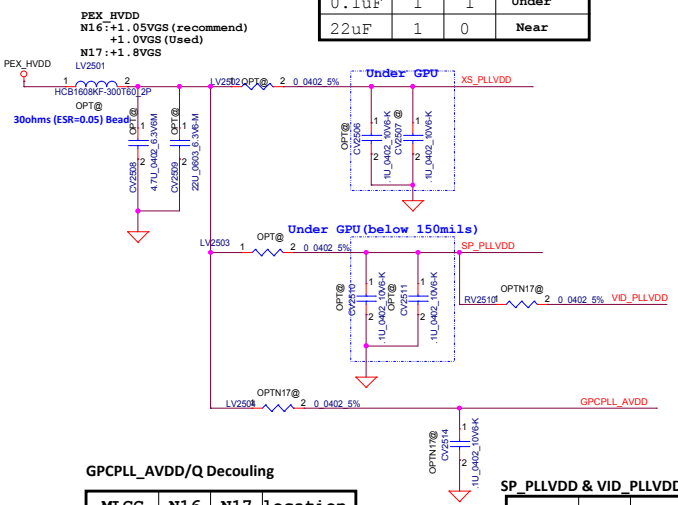


PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near

XS_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

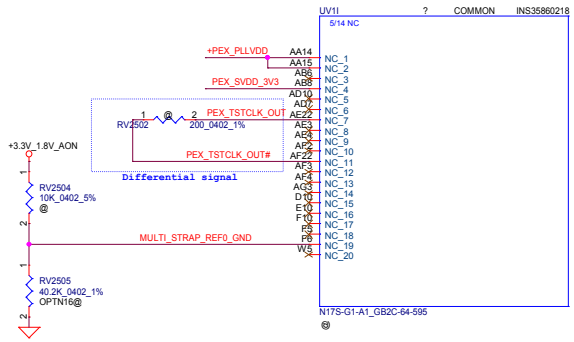


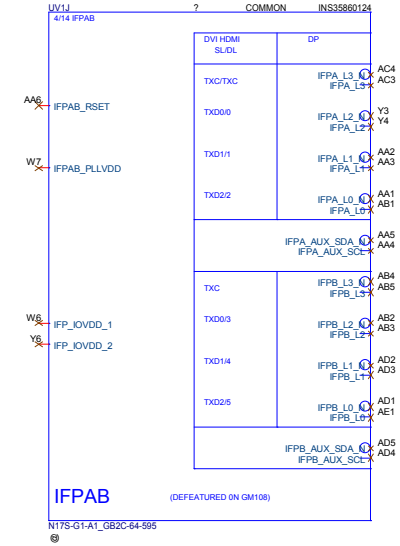
GPCPLL_AVDD/Q Decoupling

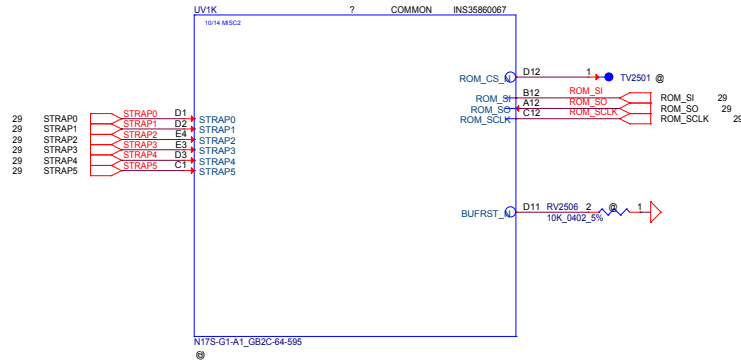
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

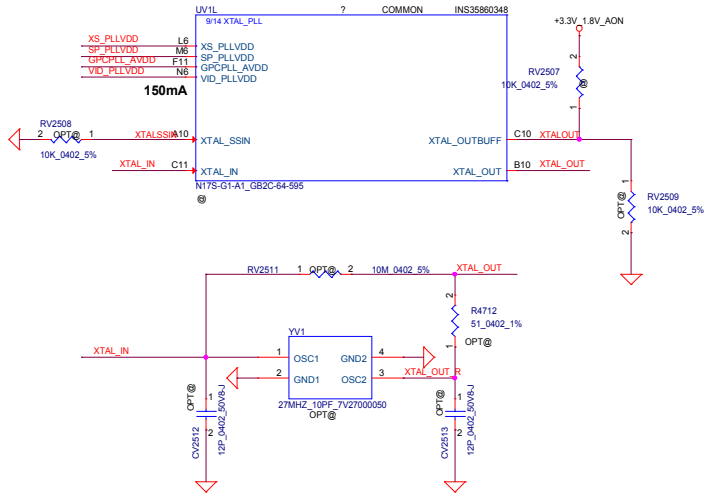
SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	









Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_STRAP/DP/HDMI

Size	Document Number	Rev
C	FS441/FS540	0.1

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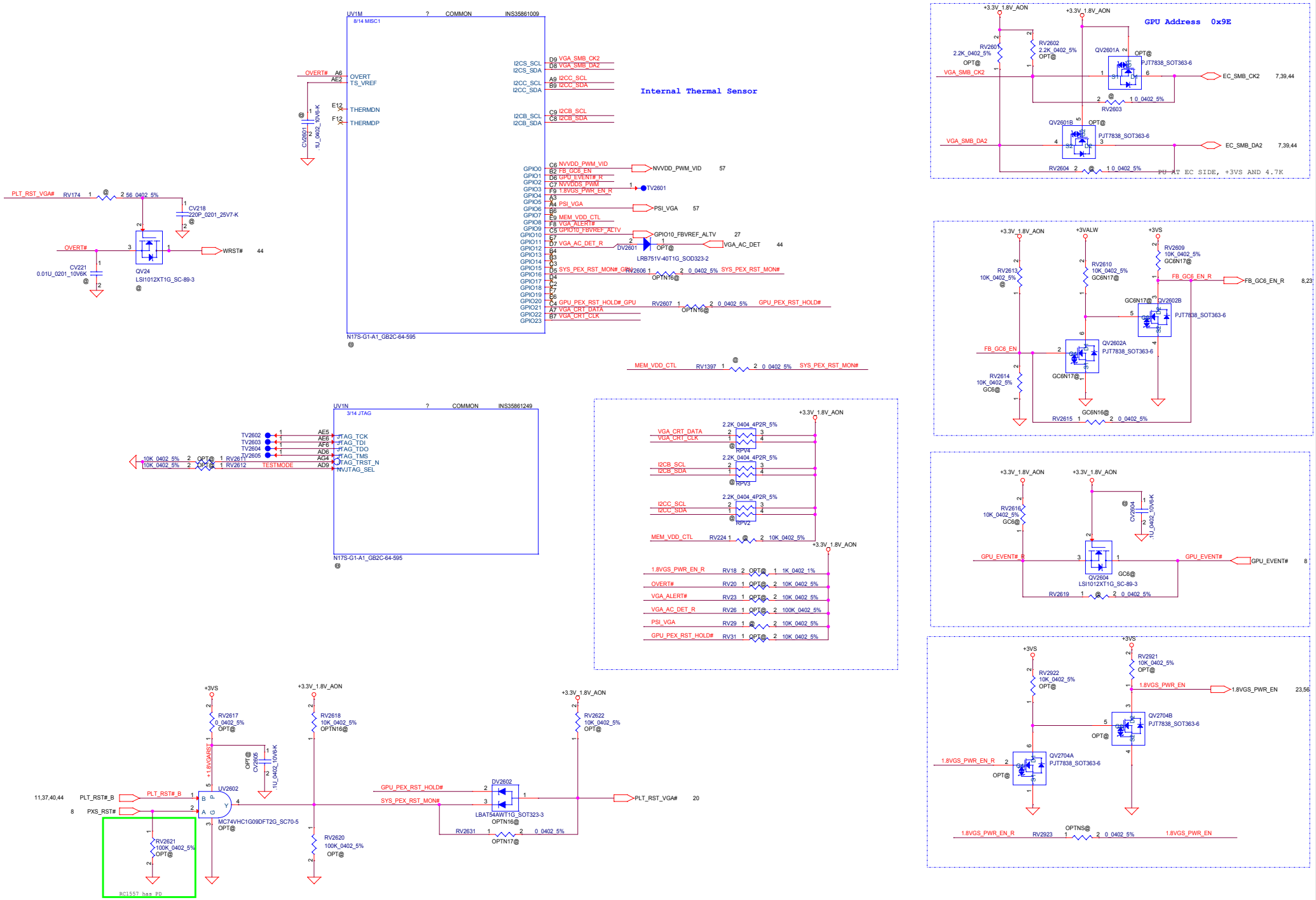

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: GPU_GPIO/JTAG

Size	Document Number	Rev
C	FS441/FS540	0.1

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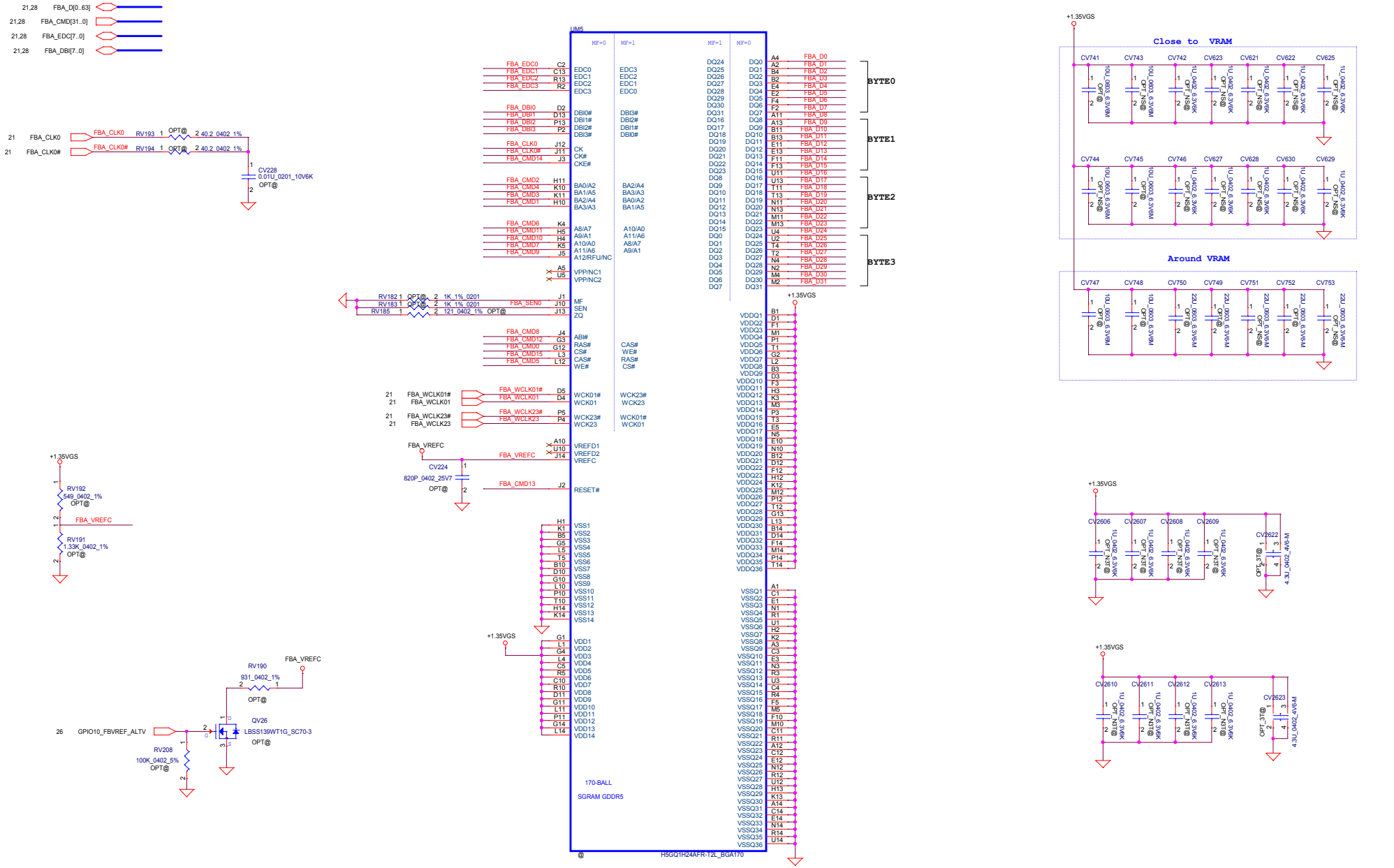
Lower 32 bits

MF=0 No Mirror

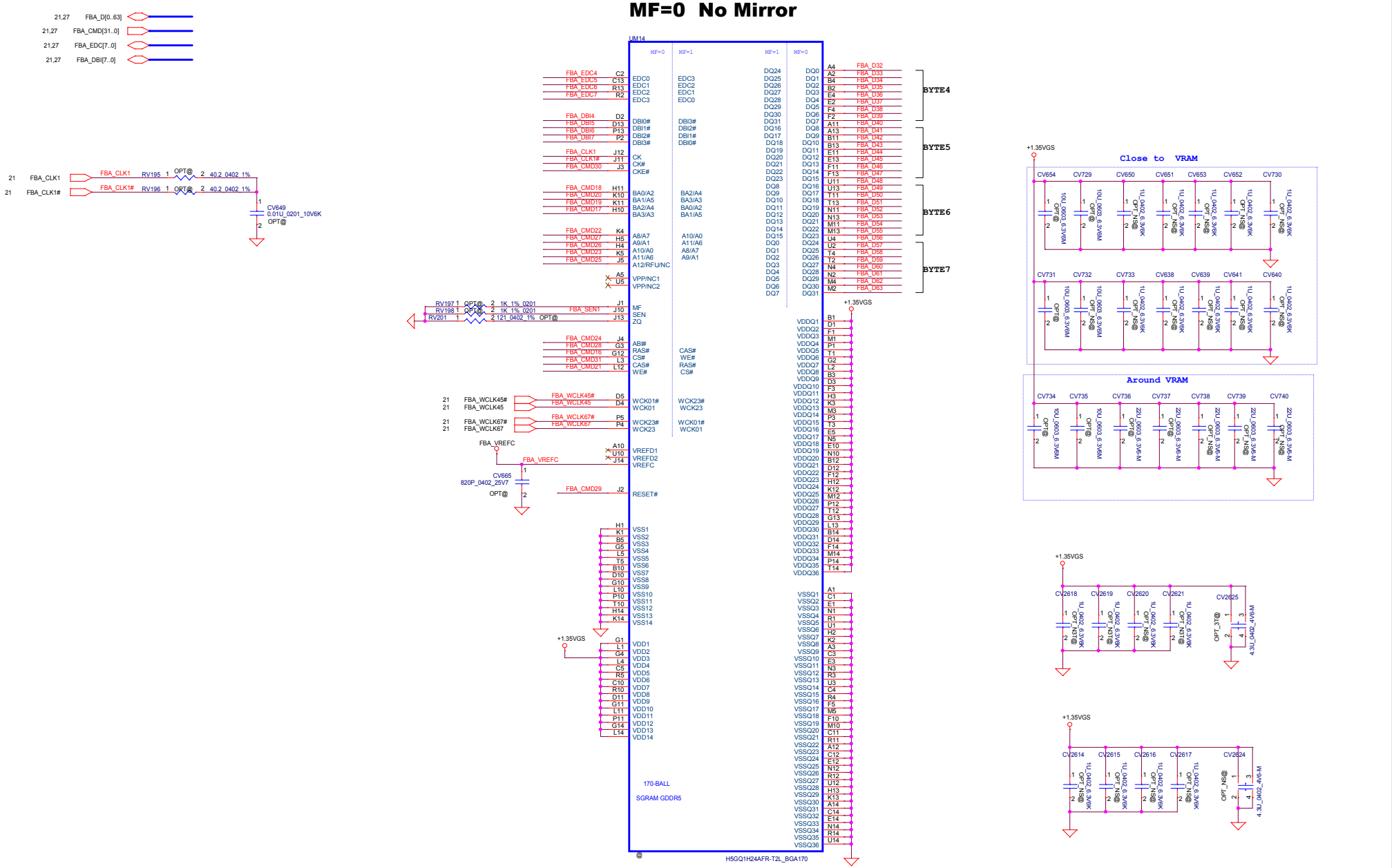


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GDDR5_Rank0_[31:0]		
Size C	Document Number FS441/FS540		Rev 0.1
Date: Wednesday, October 16, 2019	Sheet 27 of 61		

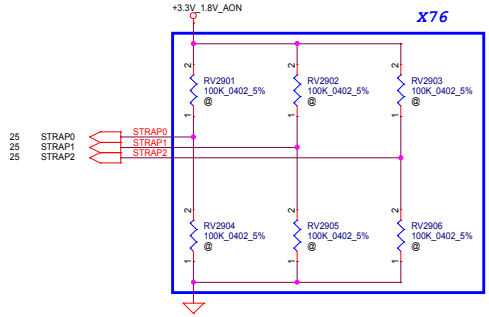
upper 32 bits

MF=0 No Mirror

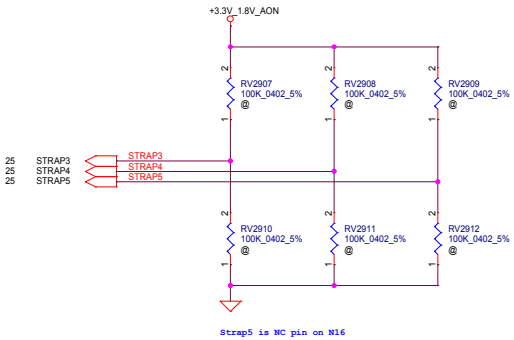


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GDDR5_Rank0_[64:32]		
Size C	Document Number FS441/FS540		Rev 0.1
Date: Wednesday, October 16, 2019	Sheet 28 of 61		



GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



Strap5 is NC pin on N16

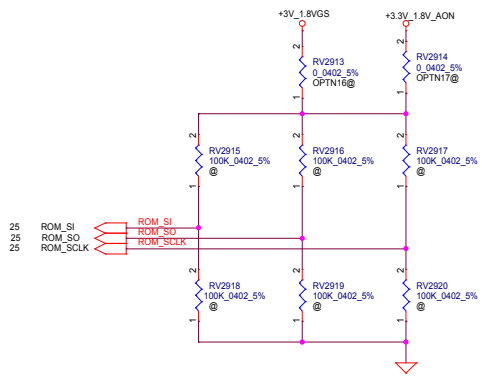
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_MISC

Size	Document Number	Rev
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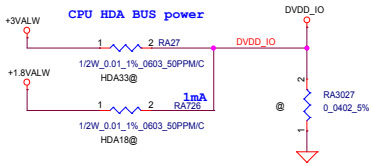
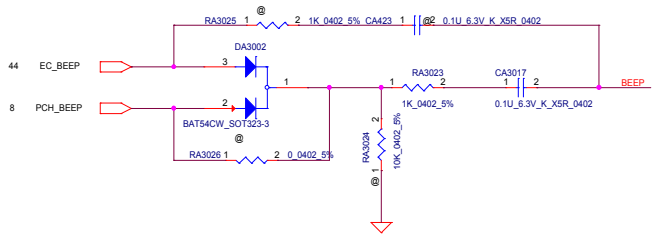
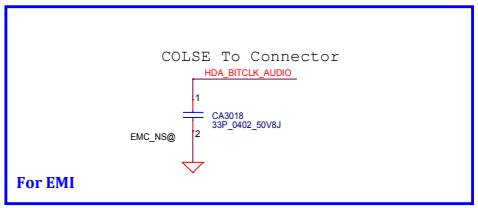
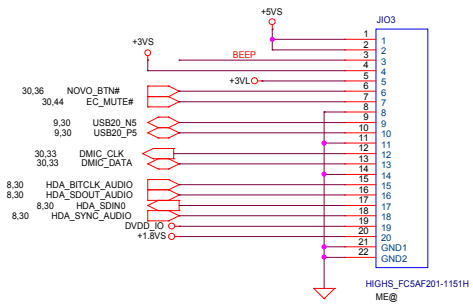
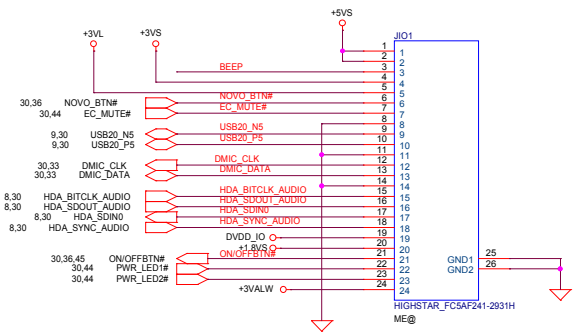




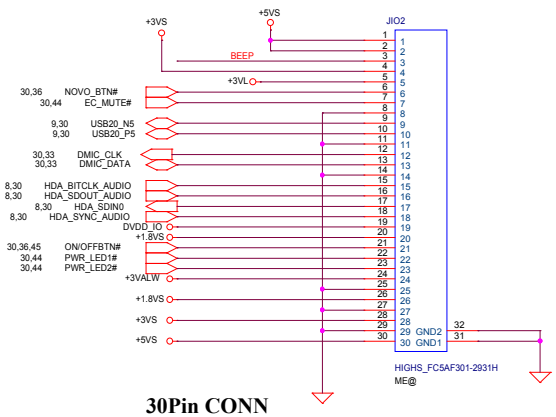




20Pin CONN



24Pin CONN



30Pin CONN

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	CODEC_RTS5199		
Size	Document Number		Rev
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Title	<Title>
Size: A	Document Number: FS441/FS540
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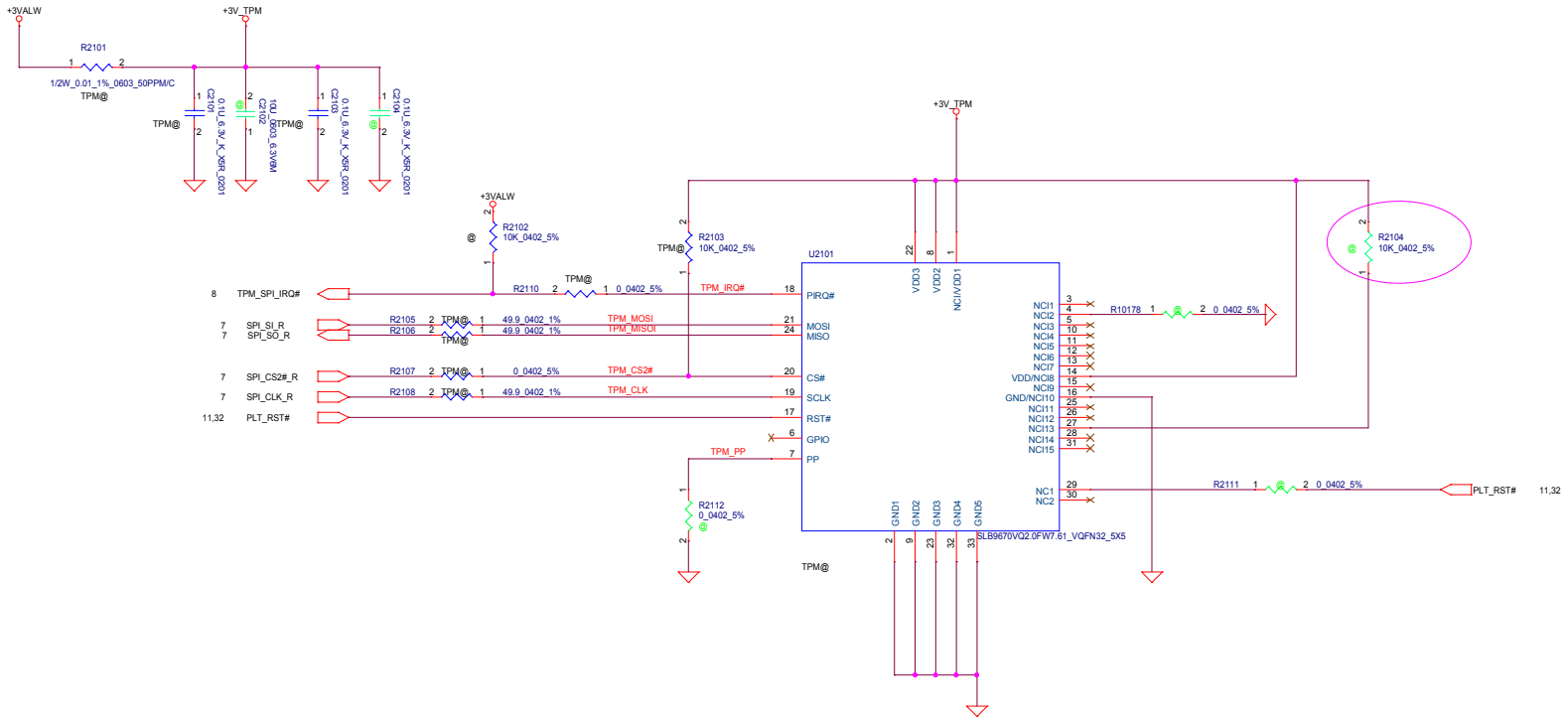
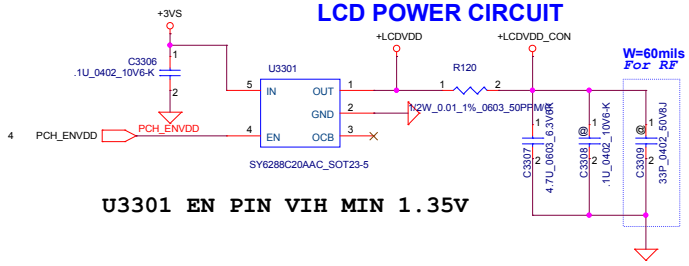


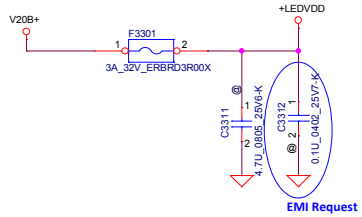
TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H330TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

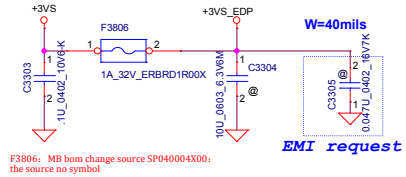
LCD POWER CIRCUIT



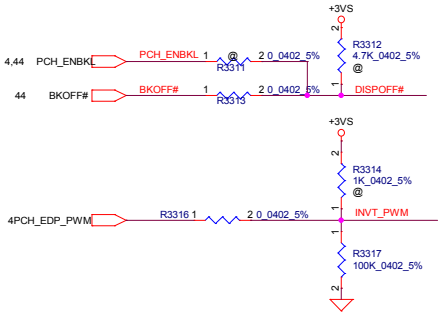
U3301 EN PIN VIH MIN 1.35V

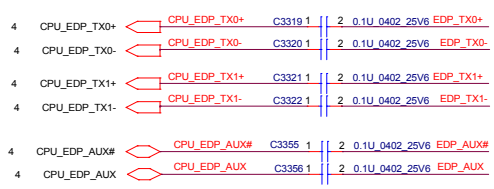


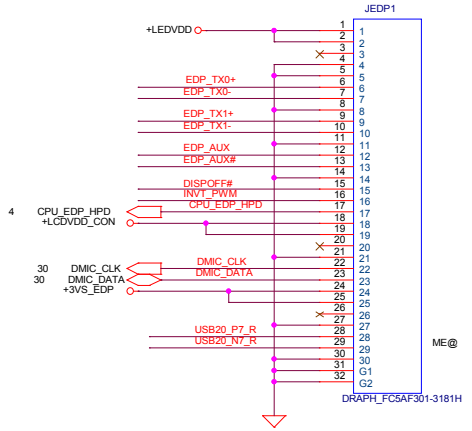
CMOS Camera

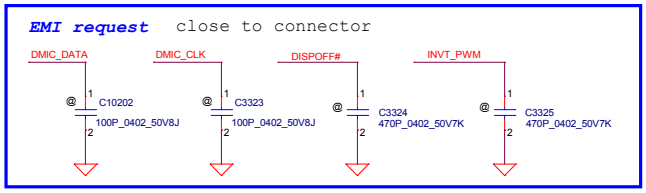


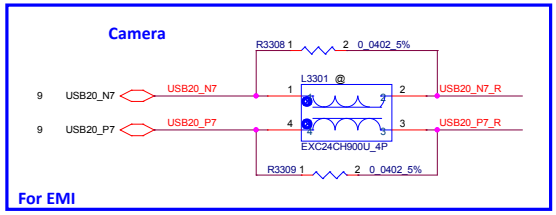
F3806: MB bom change source SP040004X00; the source no symbol



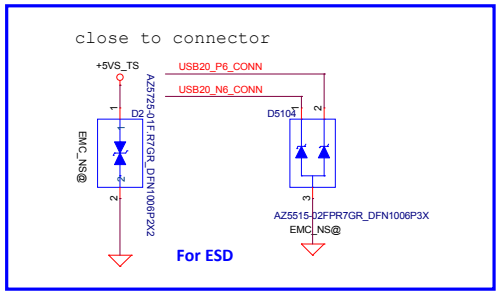


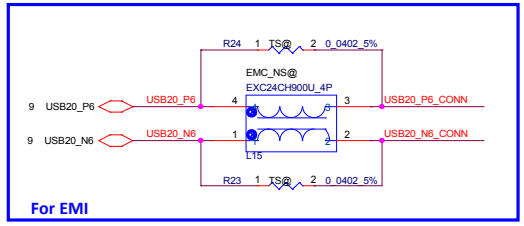


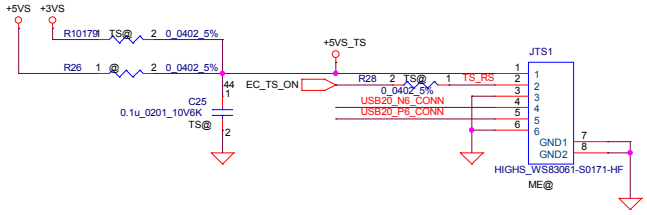




Touch Screen







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Title: **eDP/CAMERA.**

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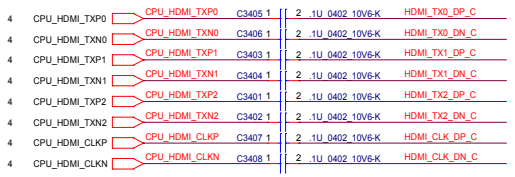

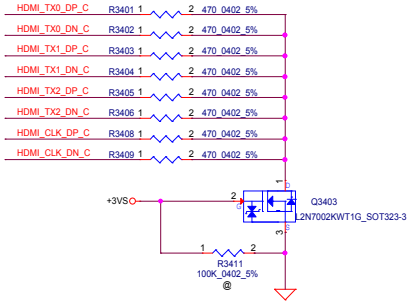

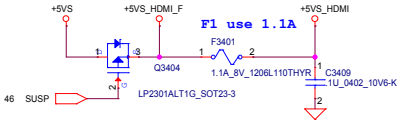

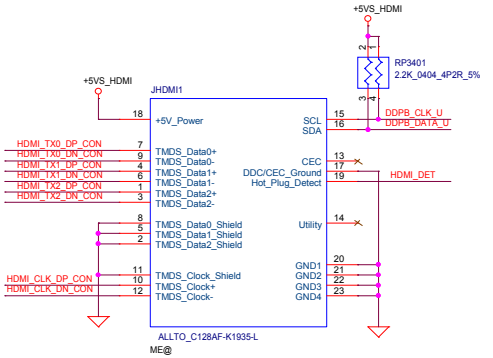

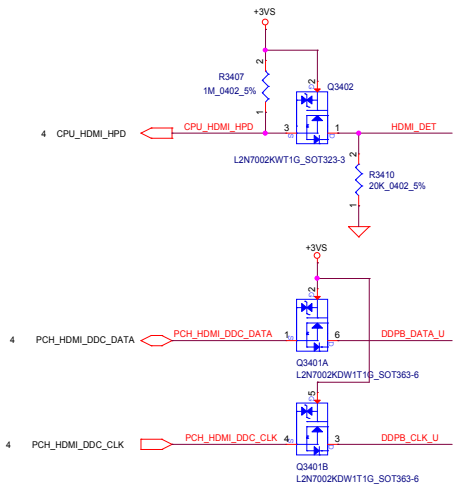

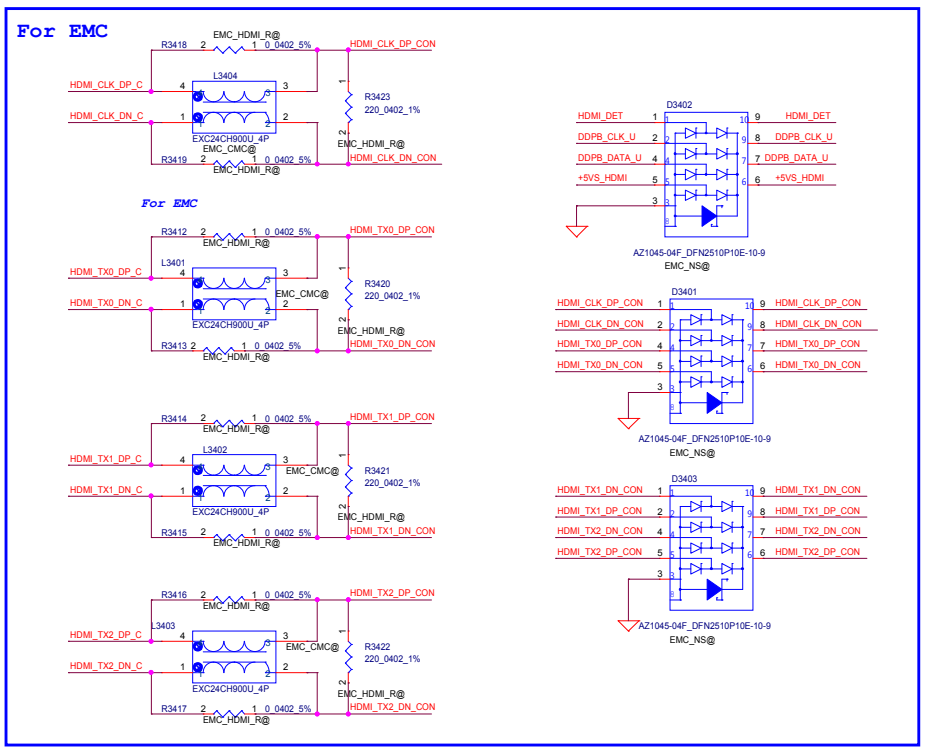

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: HDMI_CONN

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1.Project name and info update----P1

2.CE4432&CE4428&CE4429&CE4430&CE4431 Bom structure update-----P7

3.RC730 Bom structure Update(origin MP@)----P7

4.R4684&r4685 33ohm change 22ohm----P8

5.RC842 &RC3101 &Q4610 &Q4609 &RC834 BOM stucture change----P8;

6.RH829 71.5K change 75K ----P8

7.add RC3116 For PU reserve----P9

8.add RC3117 75K PD For PU GPP_F23 according PDG P484 ----P10

9.Board ID BOM stucture update----P10

10.reseve RC3118 for PM_SLP_S0# 100k PU ----P11

11.add VCCIO_SENSE&VSSIO_SENSE PU&PD Res(RC3114&RC3115) ----P13

12.C66&C67&C68&C69&C10195&C10196&C10197&C10198 0402 change 0201----P38

13.RD1712&RD1715&RD1713&RD1716&RD1742&RD1743&RD1744&RD1745 R-Short change R0402----P17

14.RD1704&RD1705 36ohm change 33ohm----P17

15.SPD link need confirm----P18

15.GPU strap need confirm----P29

17.RC3114&RC3115 0402 change 0201---P13 Id=3.2A

18.PR1607 delete---P54

19.add PC1614@ &PC1615&PC1120@&PC1121@---P54

20.Load switch swap U13---P46

21.add 17 connector Jbatt2---P52

22.PR1106&PR1101&PR1107 change 0201;
如下电容delete: PC6055; PC6053; PC6058
PC6059; PC6054
add :SB00000VT00+USM GPIO default low

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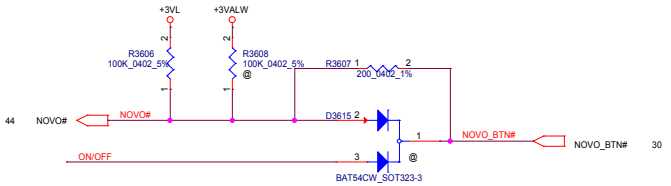
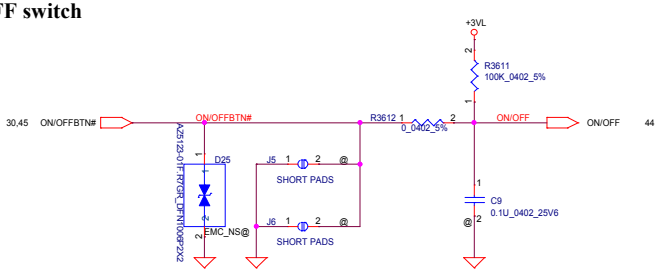
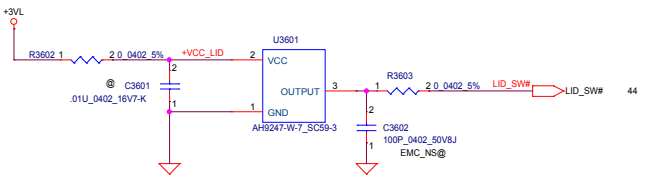
NOVO switch



ON/OFF switch



LID switch



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: HALL Sensor

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

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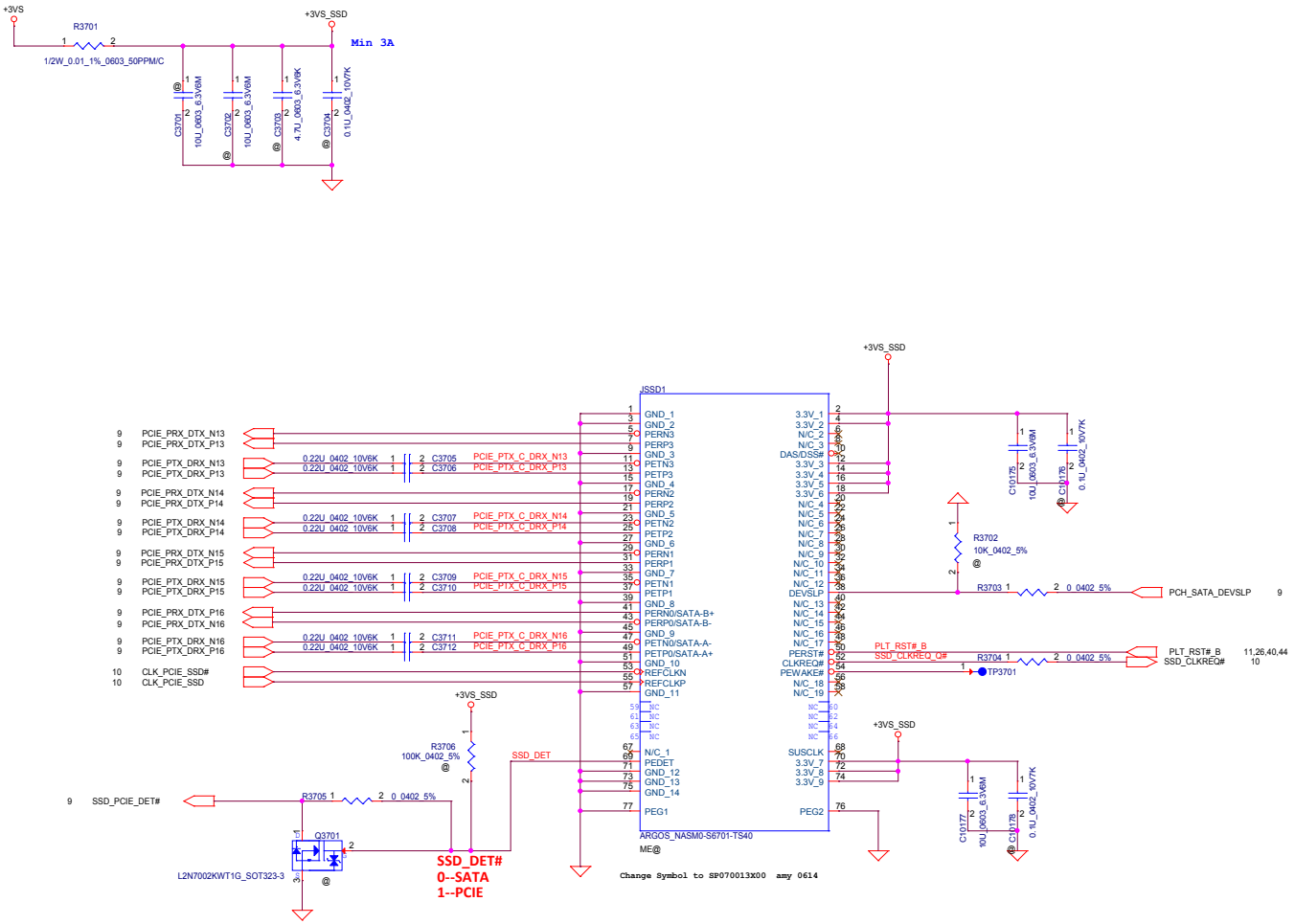

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: NGFF_SSD_1

Size	Document Number	Rev
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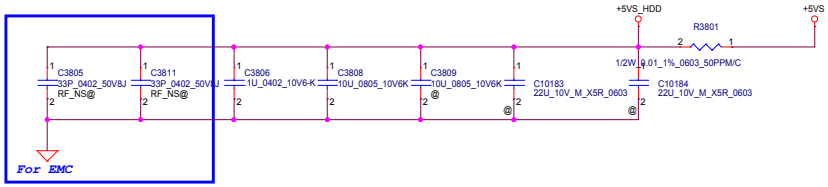

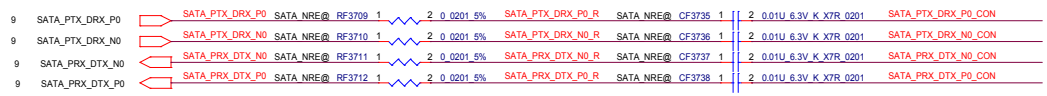

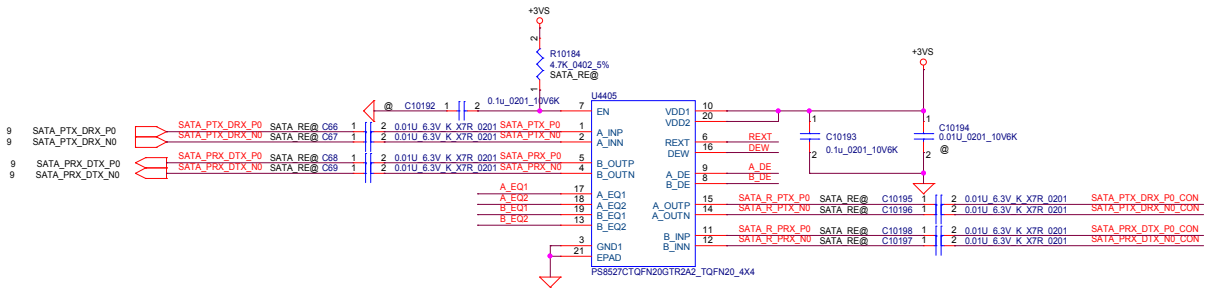

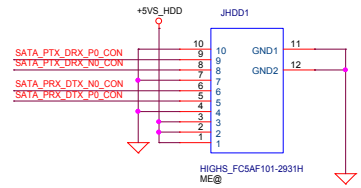

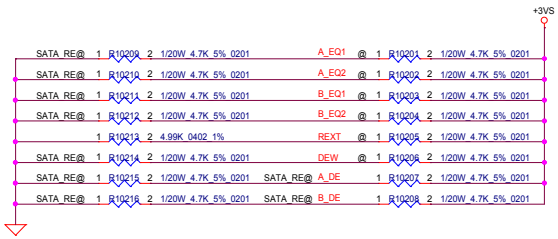

REXT: external res for output swiing adjustment
it canbe left open or tie to GND,internally generated bias
current be used and the output is as default swing setting;

the pin canbe connected 4.99k to GND,the output swing
willbe at the default value with Reference to the ex RES

DEW:De-emphasis width setting for A&B

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **SATA HDD CONN**

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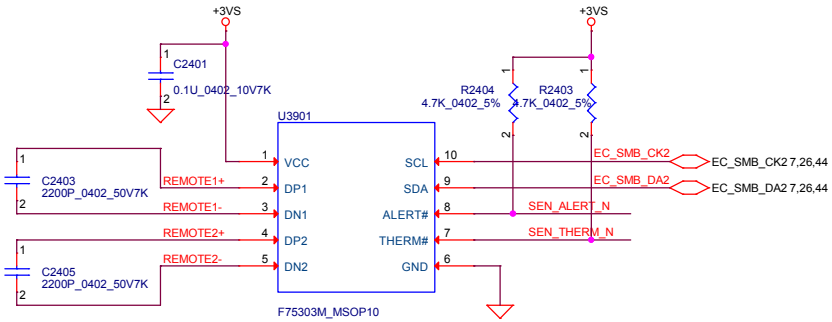
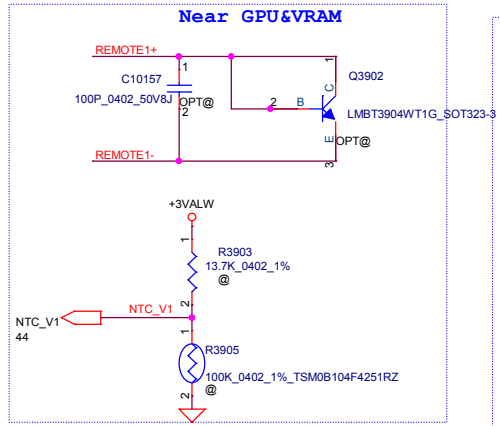
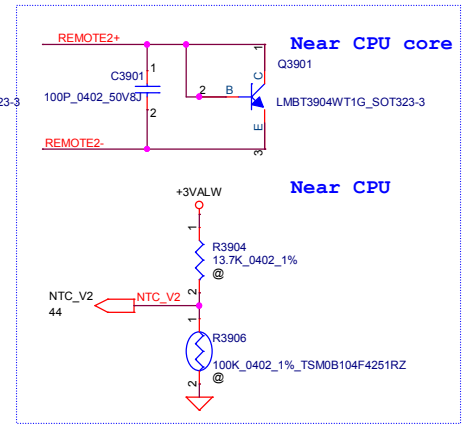
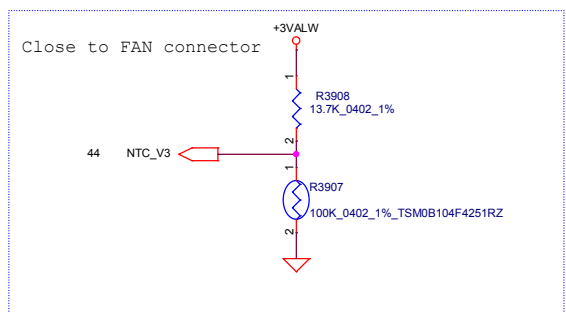
SMSC thermal sensor placed near DIMM



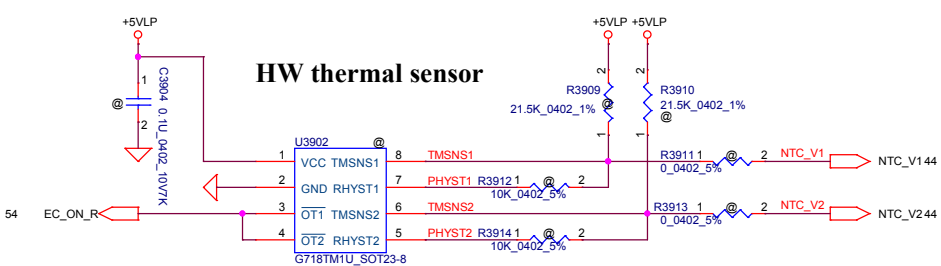
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"





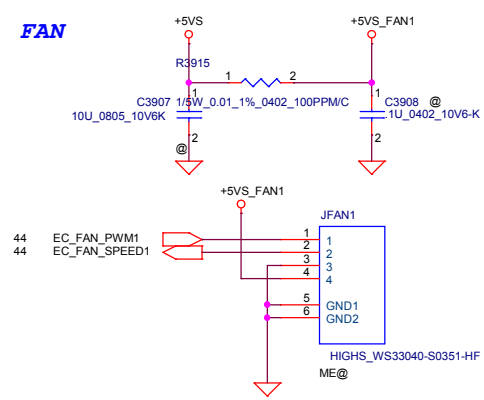


HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: **Thermal sensor/FAN CONN**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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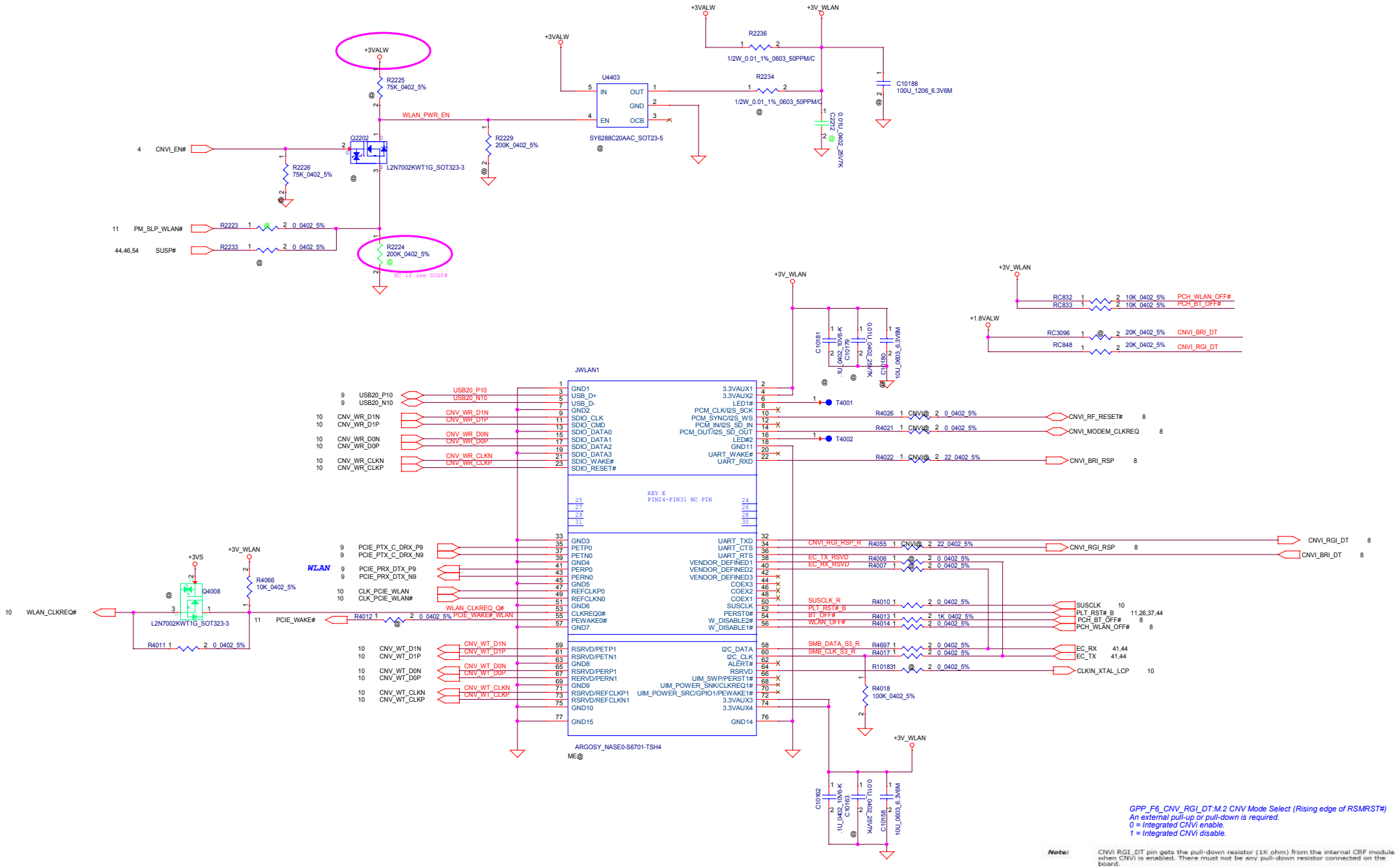
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title	NGFF_WLAN		
Size	Document Number		Rev
C	FS441/FS540		0.1
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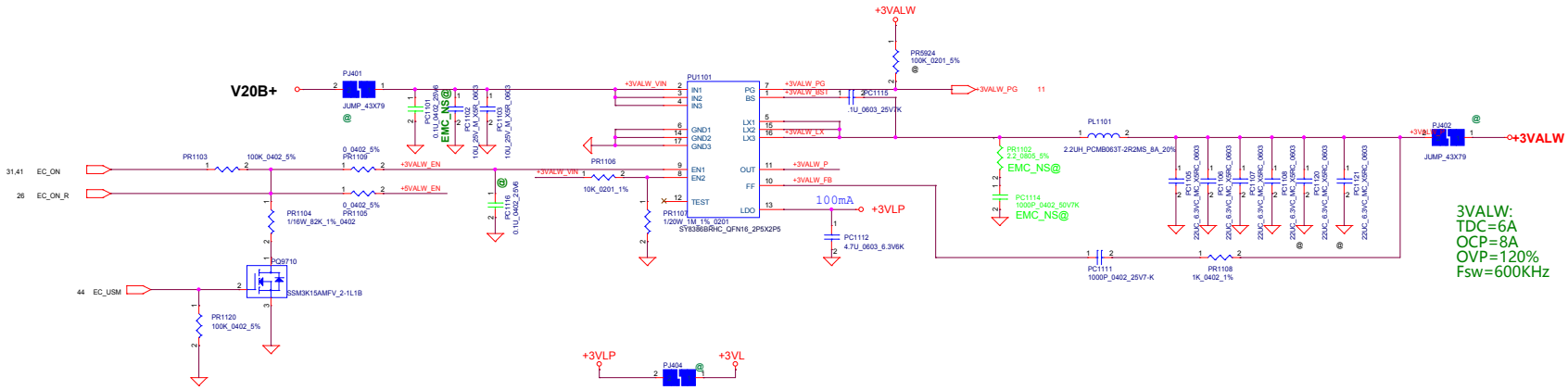
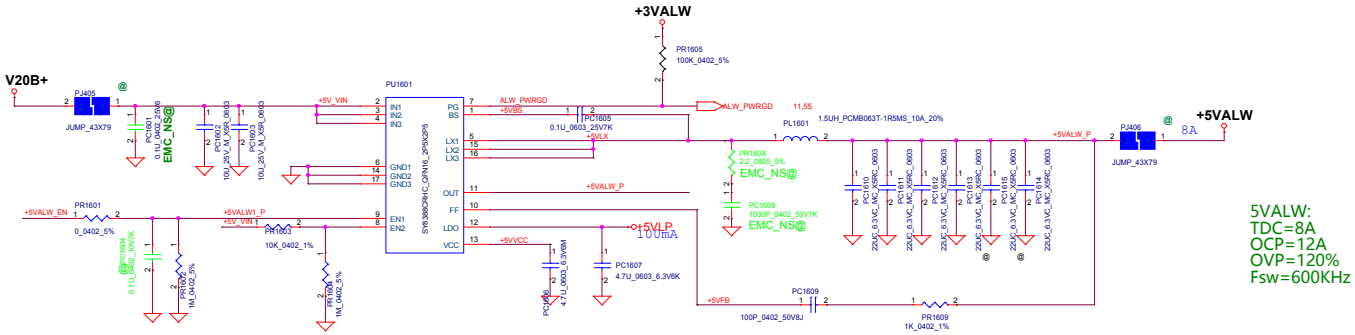
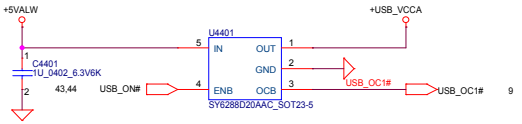




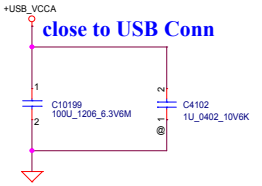
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

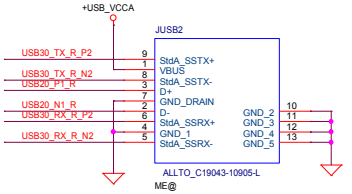
Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
Custom	S350 ADA		0.3
Date:	Wednesday, October 16, 2019	Sheet	40 of 44

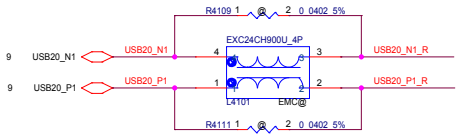
RIGHT SIDE USB3.0 PORT x1

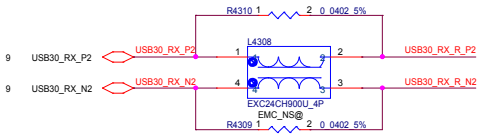


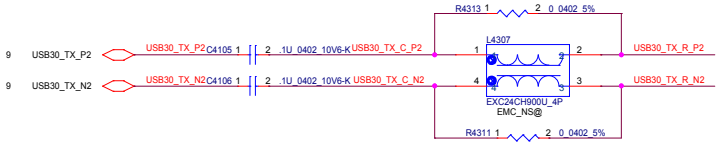
Low Active 2A



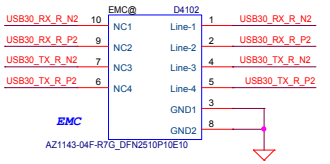




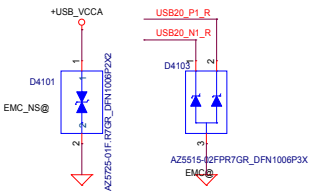




For ESD



close to USB Conn



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: USB3 PORT_LEFT

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Blank***

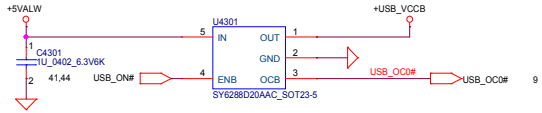
Size: Custom

Document Number: ***FS441/FS540***

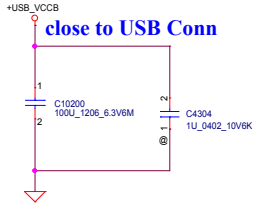
Rev: 0.1

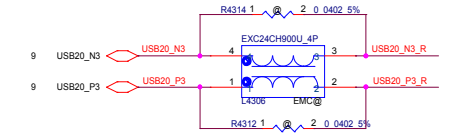
Date: Wednesday, October 16, 2019

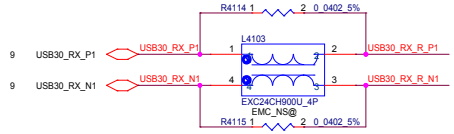
Right SIDE USB3.0 PORT

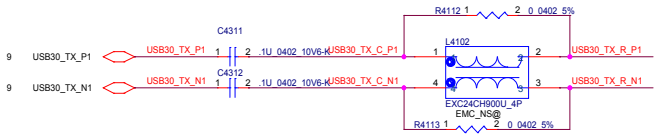


Low Active 2A

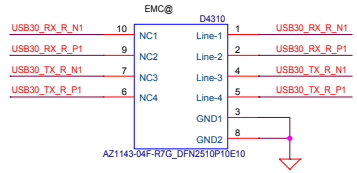




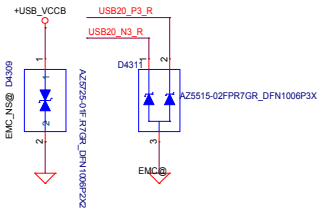


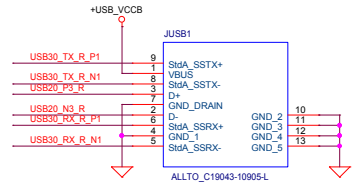


For ESD

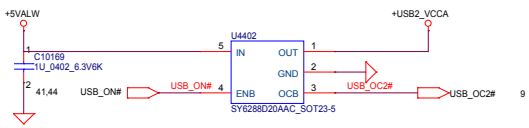


close to USB Conn

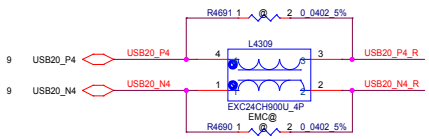




USB2.0 PORT x1

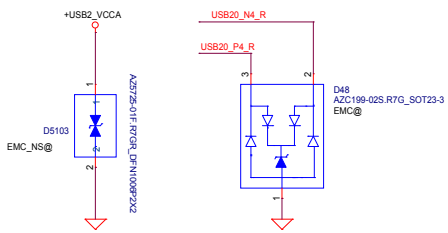


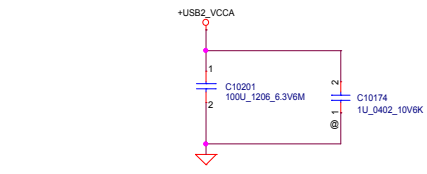
Low Active 2A

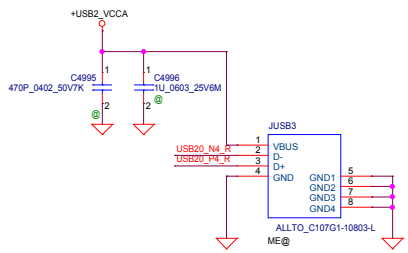


For ESD

close to USB Conn







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	USB3 Port_Right & USB2.0		
Size	Document Number		Rev
C	FS441/FS540		0.1
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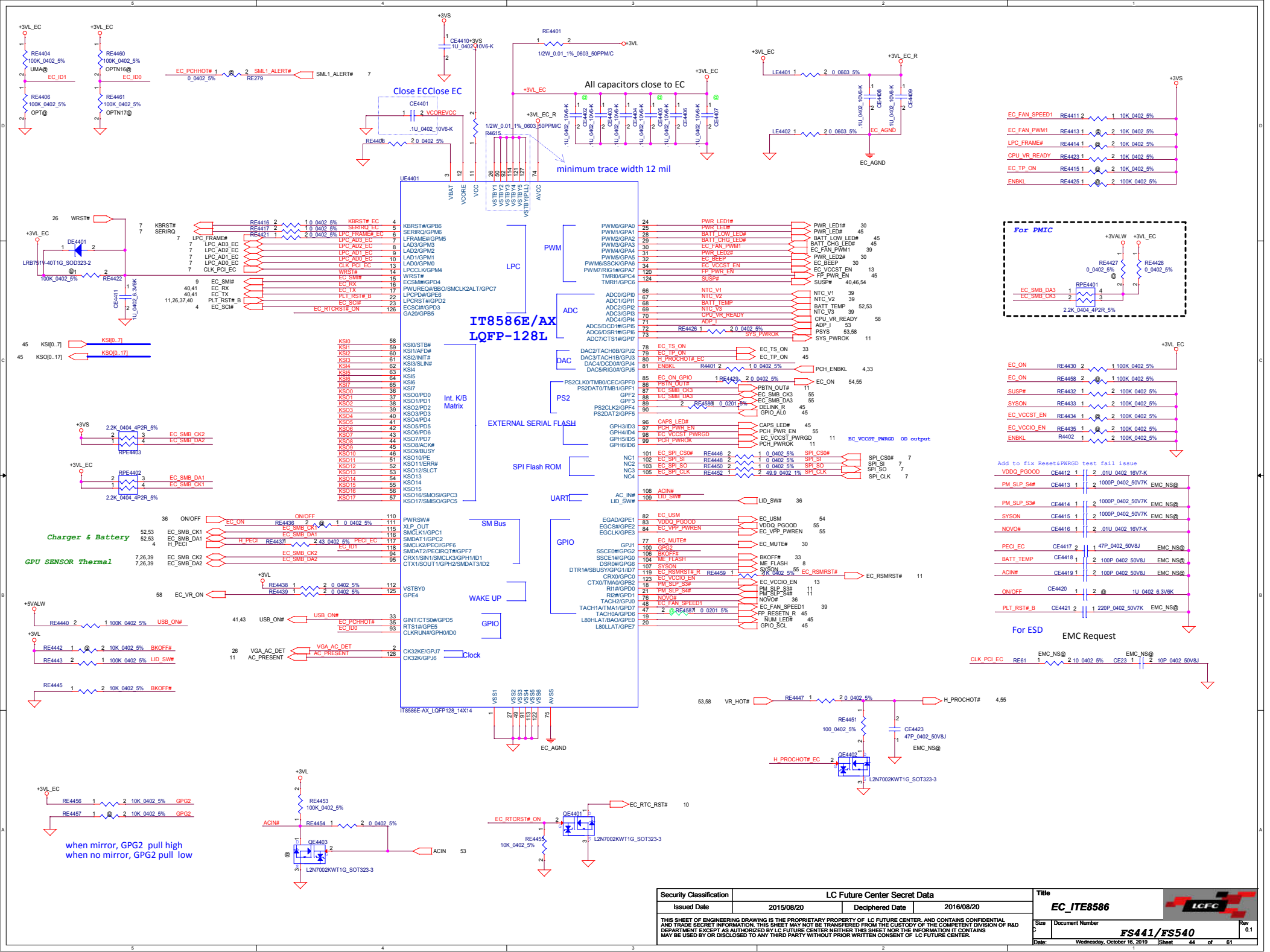
IT8586E/AX
LQFP-128L
UE4401
Close ECClose EC
All capacitors close to EC
minimum trace width 12 mil
For PMIC
For ESD
EMC Request
Add to fix Reset&PWRGD test fail issue
Charger & Battery
GPU SENSOR Thermal
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
PWM
LPC
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Int. K/B Matrix
EC_VCCST_PWRGD OD output
IT8586E-AX_LQFP128_14X14
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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Title
EC_ITE8586
Size
C
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0.1
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Wednesday, October 16, 2019
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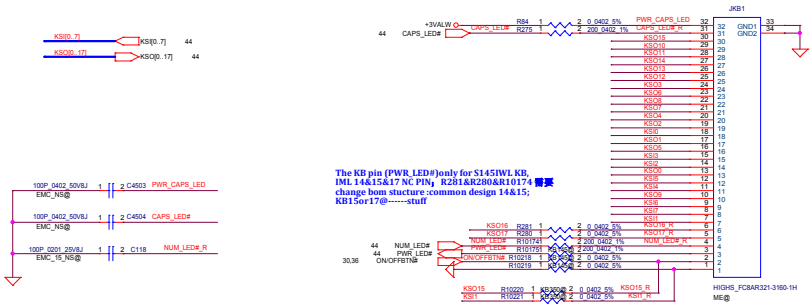
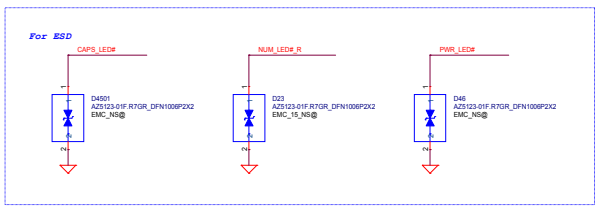
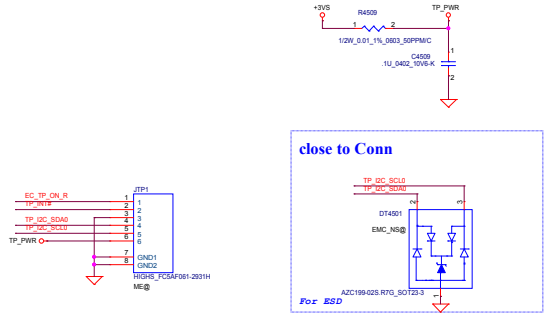
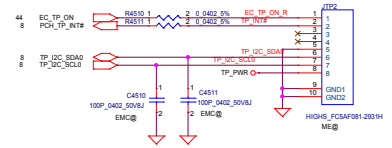
K/B Connector



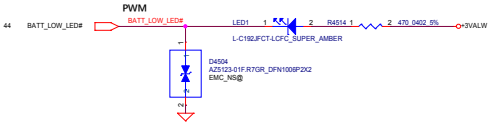


TP/B Connector

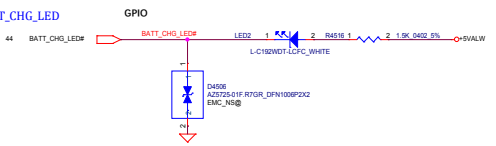


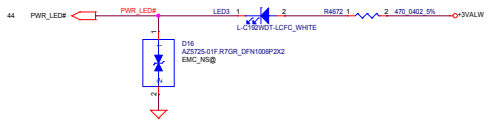


BATT_LOW_LED, Low ,Amber,if over 90%,ChG_LED(White)



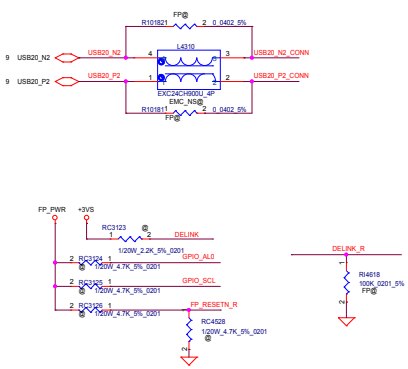
BATT_CHG_LED

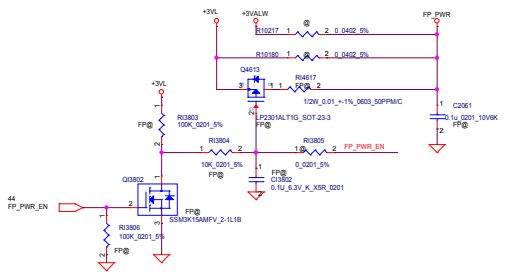


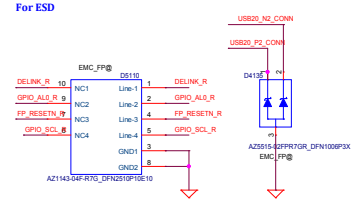


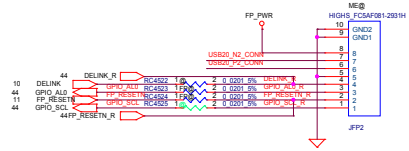
LED	Stute	LED Behavior
Power Button	System on	White_on (battery≥ 21%~100%)
		Amber_on (battery≥ 0%~20%)
	Standby LID closed	White_on (battery≥ 21%~100%)
		Amber_Blink_3S (battery≥ 0%~20%
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on (battery≥ 1%~90%)
		White_on (battery≥ 91%~100%)

Finger Print Connector









GPIO	Input/Output	S0	M5	S3	S4	S5
DELINK	Input	High	High	Low	Low	Low
GPIO_AL0	Output	1. Enrollment/Authentication (screen on): High. 2. Other: low.	Low	Low	Low	Low

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: KB/TP_CONN.

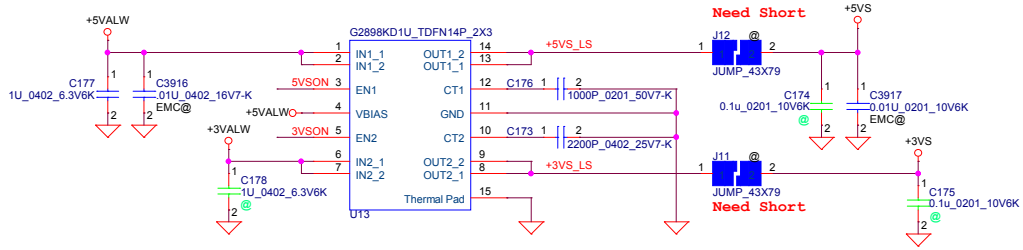
Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

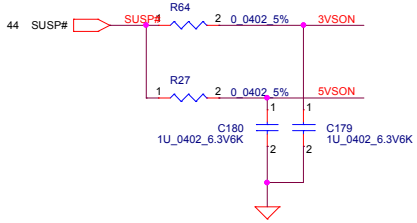
Date: Wednesday, October 19, 2016 | Sheet 45 of 61

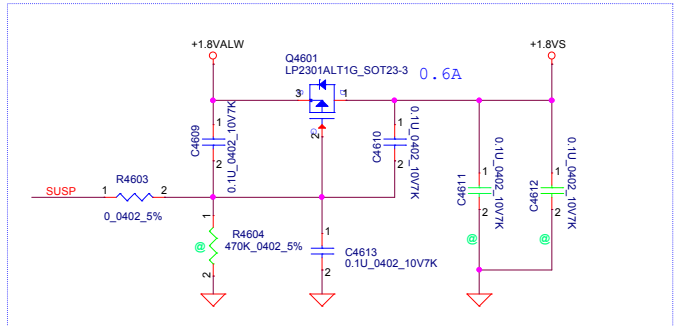
Load Switch
+5VALW To +5VS
+3VALW To +3VS

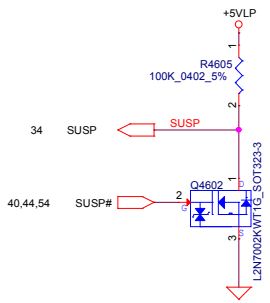
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

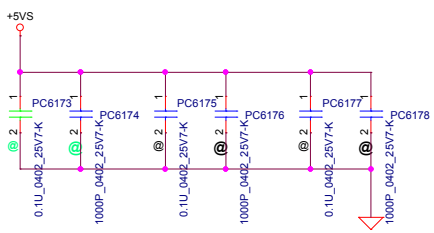


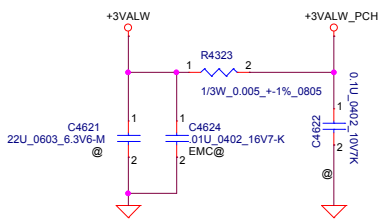


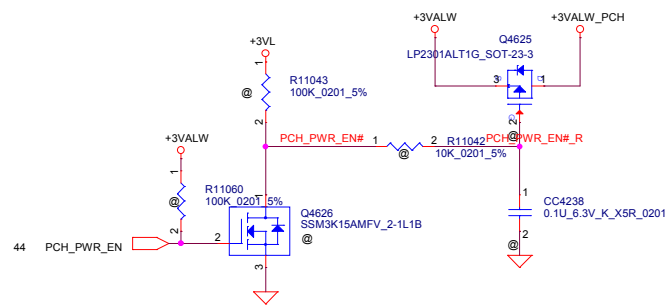




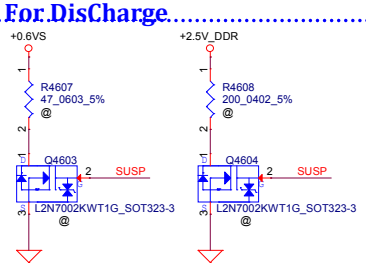
EMC demand





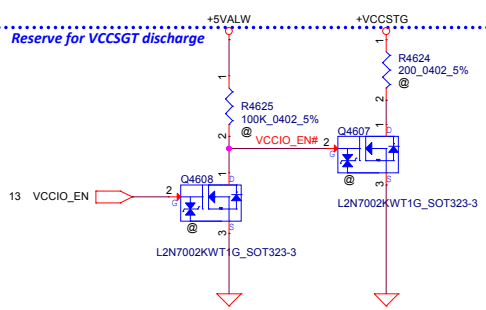


For DisCharge

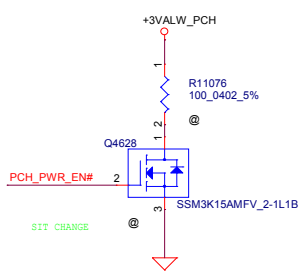


Need double check enable signal and the resistance

Reserve for VCCSGT discharge



+3VALW_PCH DISCHARGER



12.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Whiskey Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300Ω to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{discharge}$ <= VccST/VccPLL $R_{discharge}$.
3. The total capacitance on VccSTG <= total capacitance on VccST/VccPLL.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: DC V TO VS INTERFACE

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

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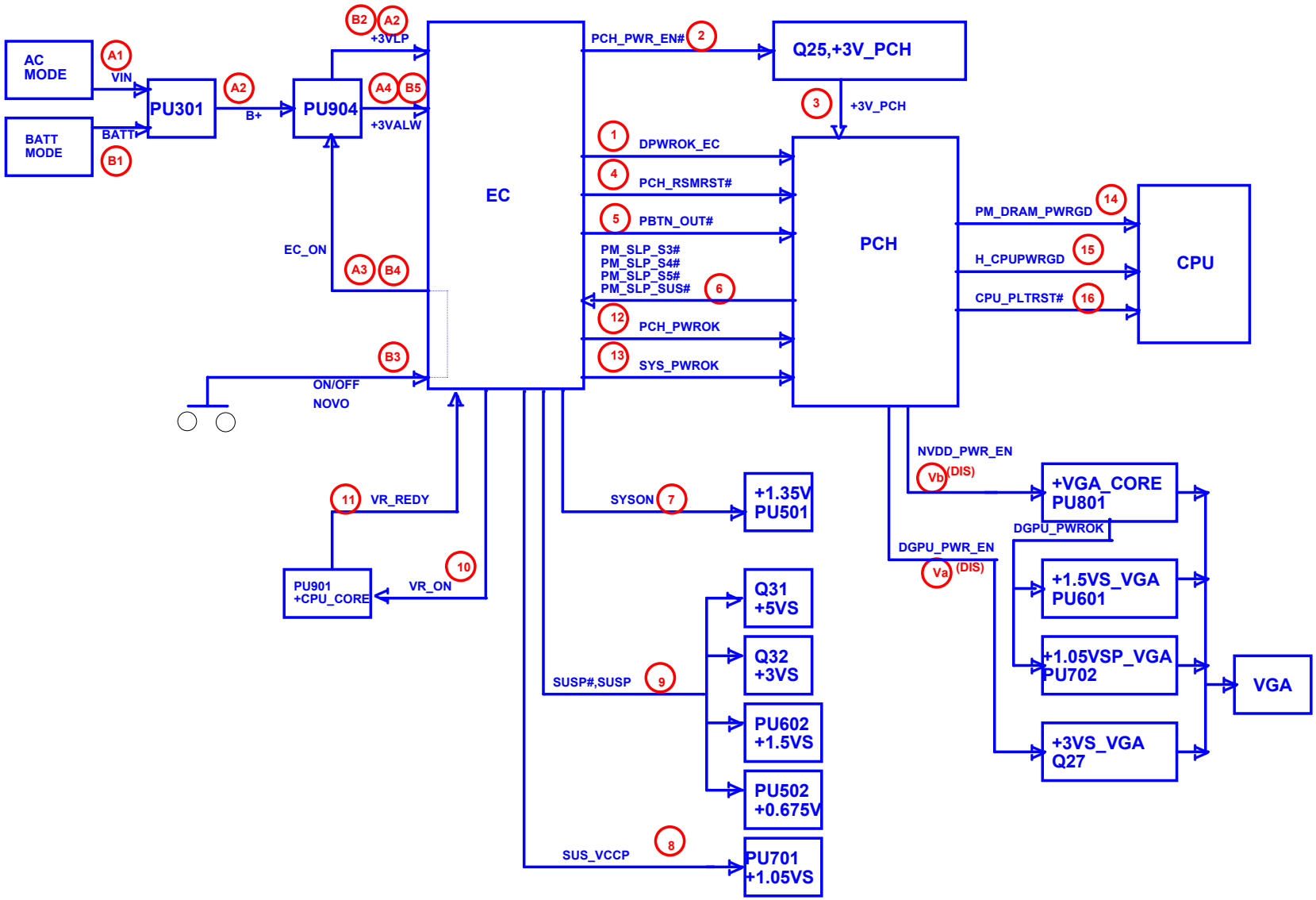

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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CPU

UC1 10510U@
Intel i7-10510U 1.8G/4C/8M
SA0000A7E00

UC1 10210U@
Intel i5-10210U 1.6G/4C/6M
SA0000A5G00

UC1 10110U@
Intel i3-10110U 2.1G/2C/4M
SA0000A7K00

UC1 6405U@
Intel 6405U 2.4G/2C/2M
SA0000AHR00

UC1 5205U@
Intel 5205U 1.9G/2C/2M
SA0000AHS00

GPU

UV1 OPTN16@
N16S-GTR-S-A2 NB
SA00007QA10

UV1 OPTN17@
N17S-G3-A1
SA0000ADH00

RV2316 OPTN17@
5.11_0805_1%
SD00001NQ00

RV2316 OPTN16@
470_0805_5%
SD00247008J

OPTN16@
RV2313
30K_0402_5%
SD02830028J

OPTN17@
RV2313
10K_0402_5%
SD02810028J

PCB_MB

ZZZ1 GS452@
NM-C781
DA600016S00

ZZZ10 GS552@
NM-C781
DA600016S00

ZZZ11 GS752@
NM-C781
DA600016S00

ZZZ6 SAM_VR_N16@
V2G SAM N16
X7648812005

ZZZ12 SAM_VR_N17@
V2G SAM N17
X7648A12003

VRAM_Samsung

ZZZ5 Hyn_VR_N16@
HYNIX V2G N16S
X7648912001

ZZZ13 Hyn_VR_N17@
HYNIX V2G N17S
X7648812006

VRAM_Hynix

ZZZ4 Mic_VR_N16@
V2G MIC N16
X7648A12002

ZZZ14 Mic_VR_N17@
V2G MIC N17
X7648812007

VRAM_Micron

ZZZ9 SAM_DRAM@
D4G SAM
X7648812008

DRAM_Samsung

ZZZ8 Hyn_DRAM@
HYNIX D4G
X7648812009

DRAM_Hynix

ZZZ7 Mic_DRAM@
D4G MIC
X7648812003

DRAM_Micron

SO_DIMM only

RC805 NMD@
SO_DIMM
SD02810028J

RC812 NMD@
SO_DIMM
SD02810028J

RC811 NMD@
SO_DIMM
SD02810028J

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *Virtual symbol*

Size	Document Number	Rev
C	FS441/FS540	0.1

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Hole

H2
HOLEA
PAD_C10P0D8P0

PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

MD Shielding

SH1 SPRING_FINGER_6.2X1.64
SH2 SPRING_FINGER_6.2X1.64
SH3 SPRING_FINGER_6.2X1.64
SH4 SPRING_FINGER_6.2X1.64
SH5 SPRING_FINGER_6.2X1.64
SH6 SPRING_FINGER_6.2X1.64

H3 HOLEA PAD_CT7P0B6P0D3P2
H4 HOLEA PAD_CT7P0B6P0D3P2
H5 HOLEA PAD_CT7P0B6P0D3P2
H6 HOLEA PAD_CT7P0B6P0D3P2
H7 HOLEA PAD_CT7P0B6P0D3P2
H8 HOLEA PAD_CT7P0B6P0D3P2

H9 HOLEA PAD_C7P0D4P0
H10 HOLEA PAD_C7P0D4P0

H17 HOLEA PAD_O2P5X3P0D2P5X3P0N
H18 HOLEA PAD_O2P5X3P0D2P5X3P0N

SODIMM Shielding

SH10 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 SHIELDING_SUL-35A2M_9P2X3P3_1P

H11 HOLEA PAD_C7P0D2P8
H12 HOLEA PAD_C7P0D2P8
H13 HOLEA PAD_C7P0D2P8

H14 HOLEA PAD_C7P0D2P4

HICT1 HOLEA PAD_C2P5D2P5N
HICT2 HOLEA PAD_C2P5D2P5N

H15 HOLEA PAD_CT7P0B10P0D4P0
H16 HOLEA PAD_CT7P0B10P0D4P0

HICT3 HOLEA PAD_C2P5D2P5N

Title			
Hole			
Size B	Document Number FS441/FS540		Rev 0.1
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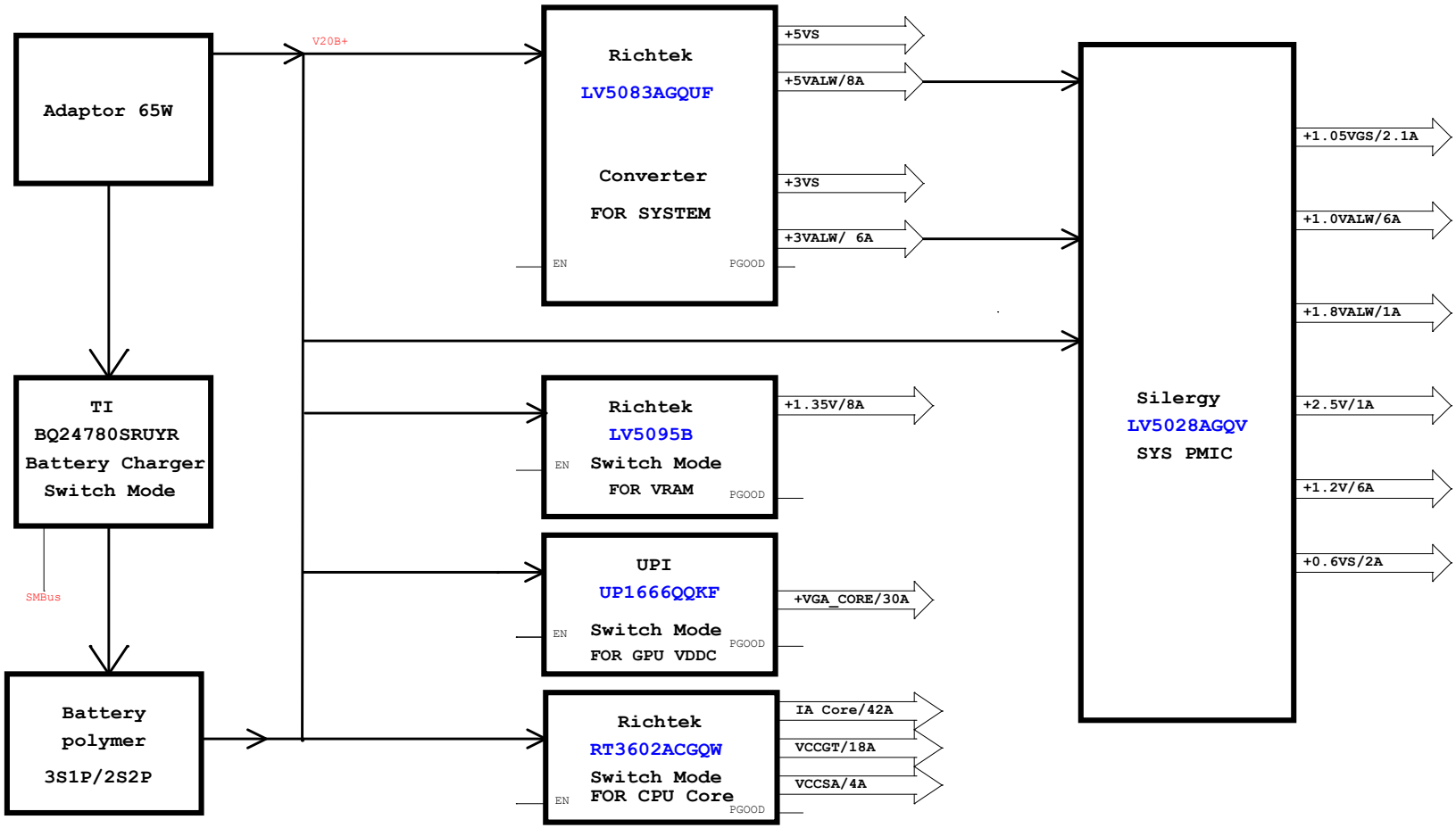

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-Power Diagram

Size	Document Number	Rev
C	140S-WHL	0.3

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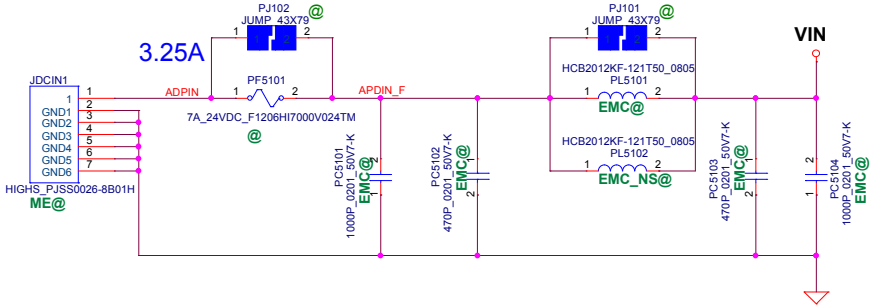
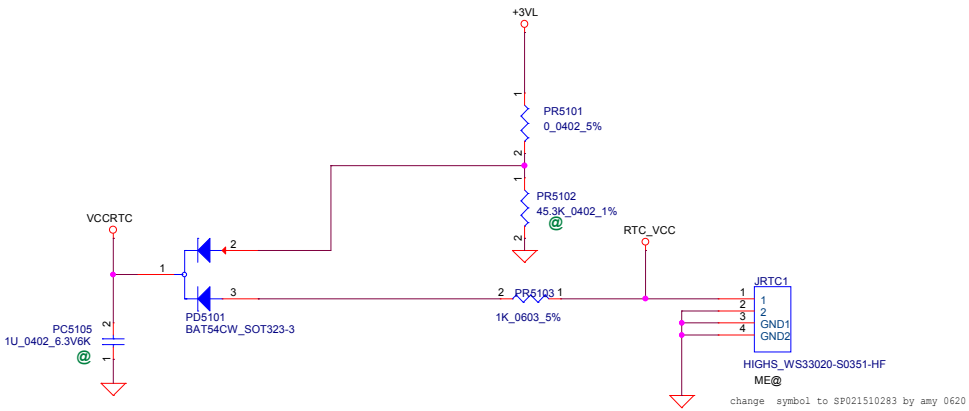


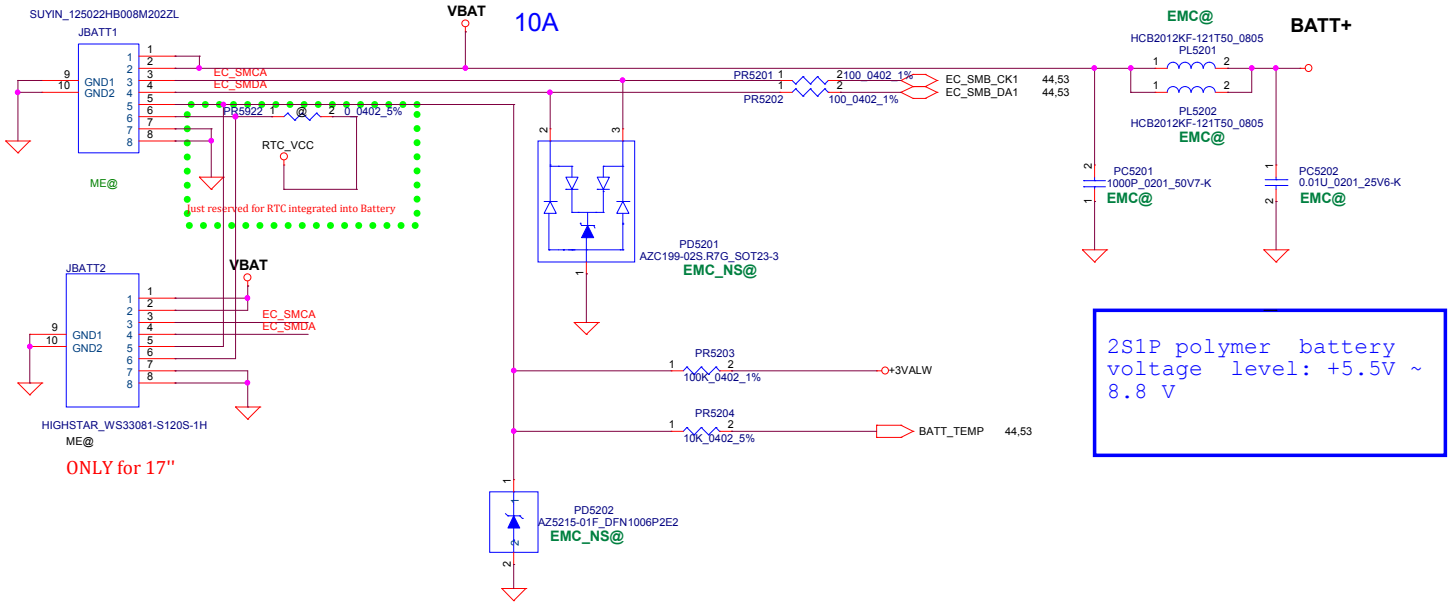


RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size: Custom	Document Number: 140S-WHL	Rev: 0.3
Date: Wednesday, October 16, 2019	Sheet 51 of 61	

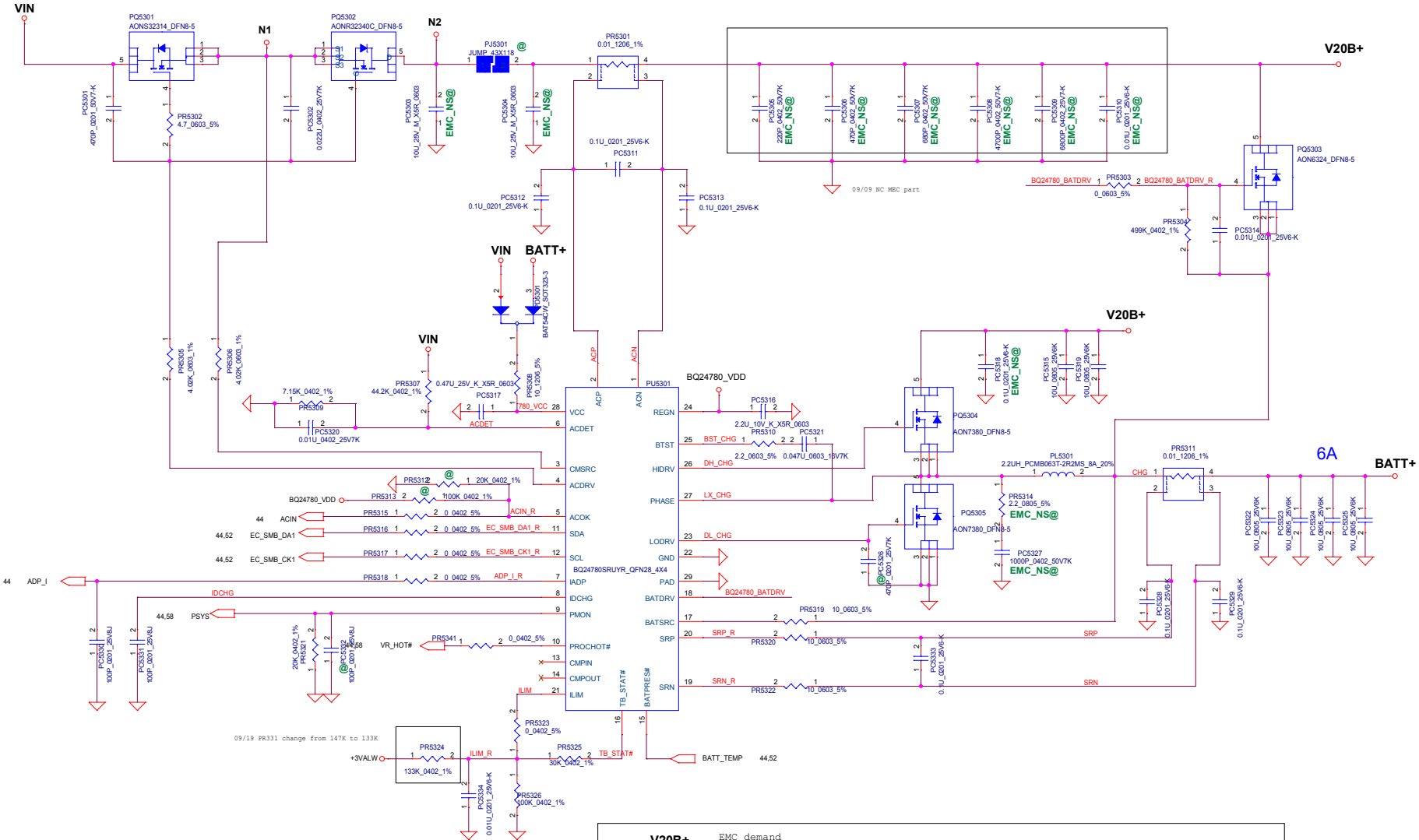


Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	140S-WHL	0.3

Date: Wednesday, October 16, 2019 Sheet 52 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: **PWR-CHARGER**

Size	Document Number	Rev
C	140S-WHL	0.3

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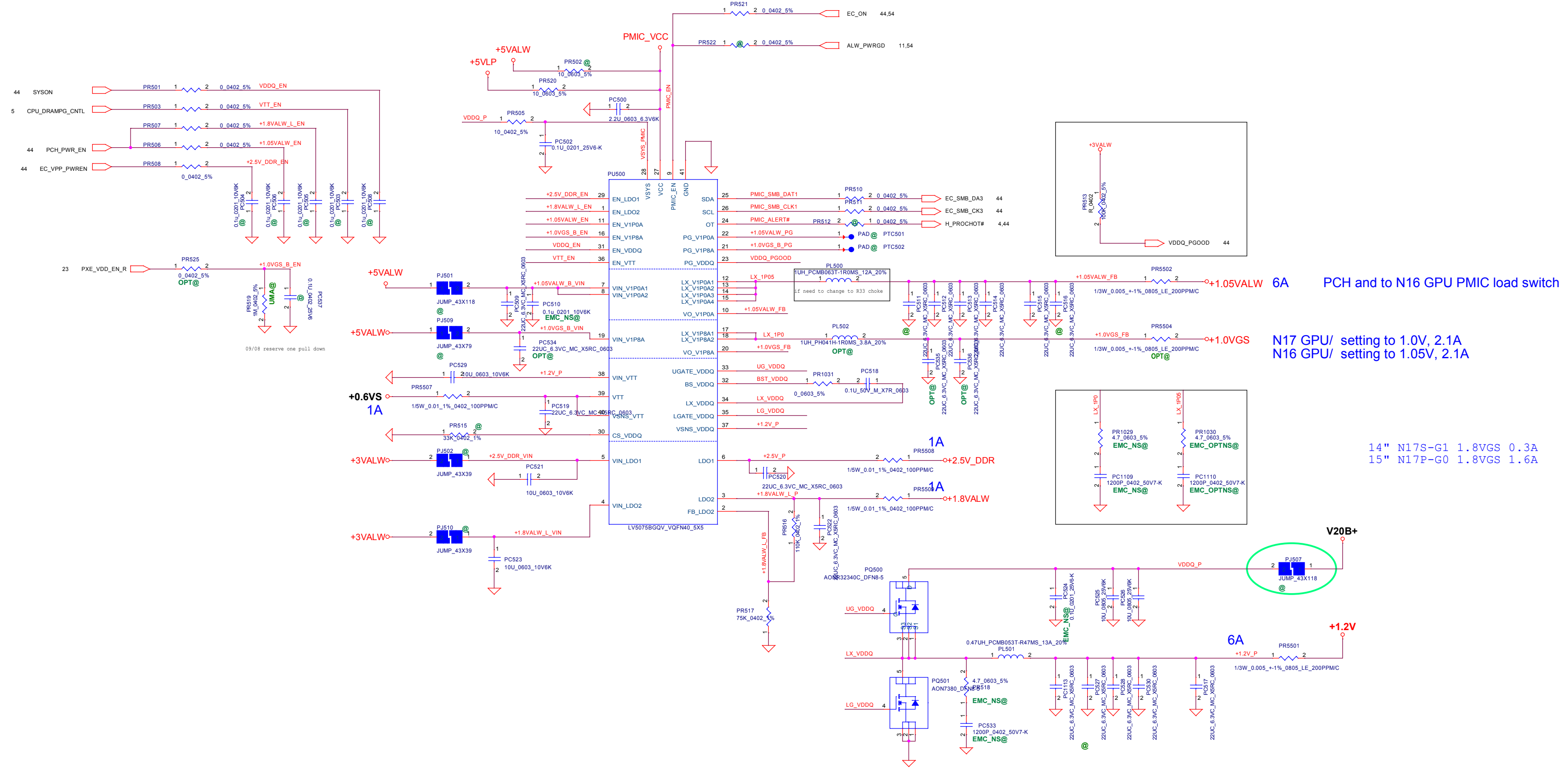

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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Title: PWR PMIC-DDR4/1.0ALW/1.8ALW

Size: Custom | Document Number: 140S-WHL | Rev: 0.3

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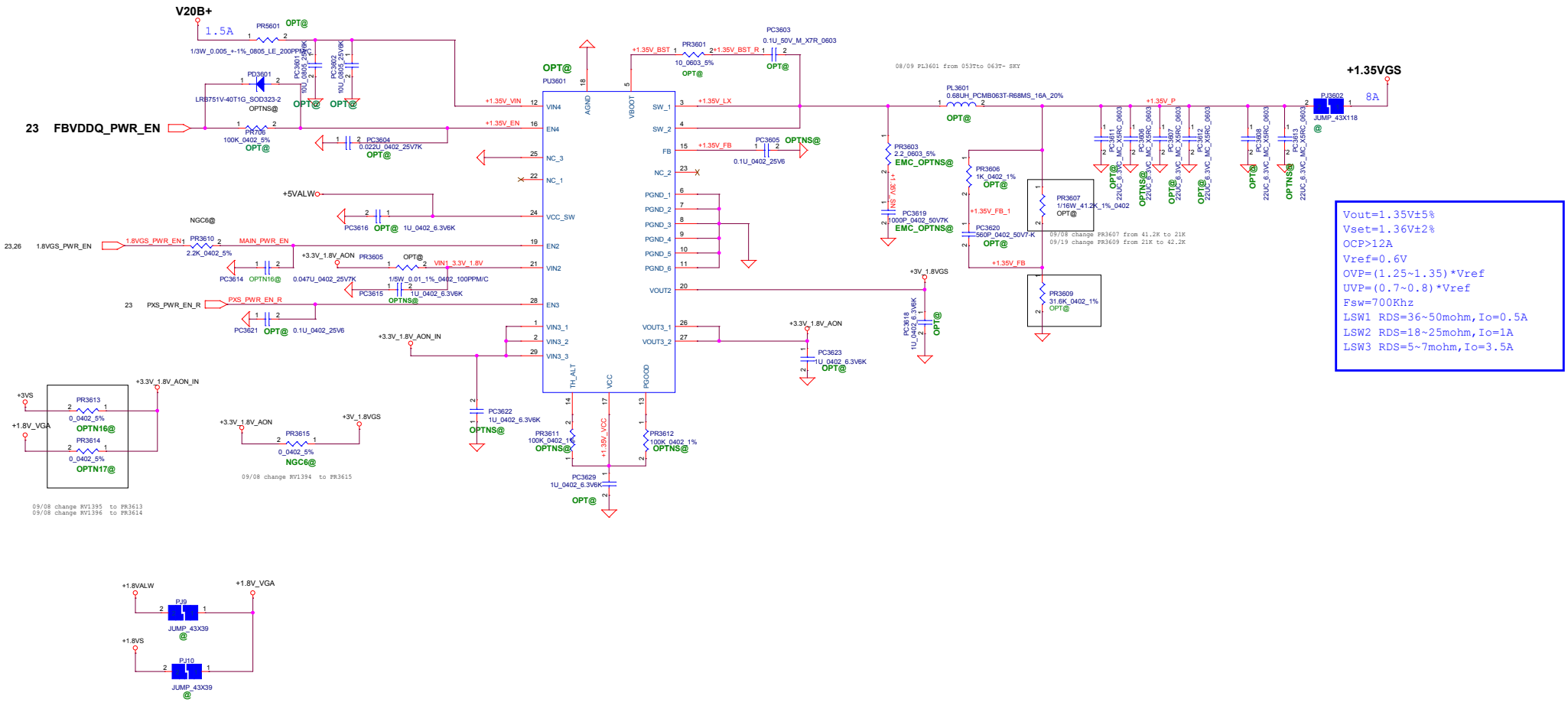

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-VGA-PMIC
Size: Custom	Document Number: 140S-WHL
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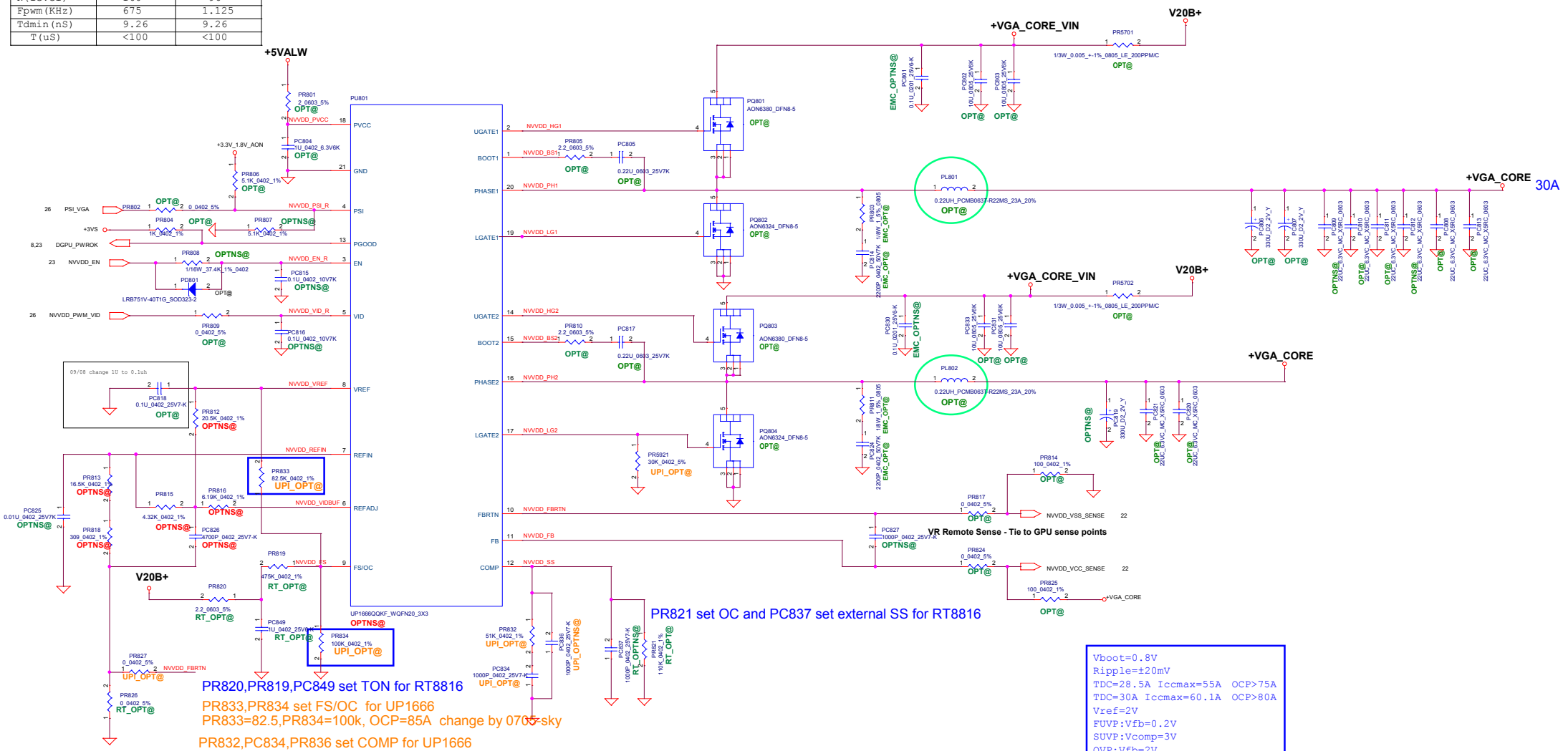
PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



Vboot=0.8V
Ripple=±20mV
TDC=28.5A Iccmax=55A OCP>75A
TDC=30A Iccmax=60.1A OCP>80A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=320KHz

PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-VGA_CORE		
Size: Custom	Document Number: 140S-WHL		Rev: 0.3
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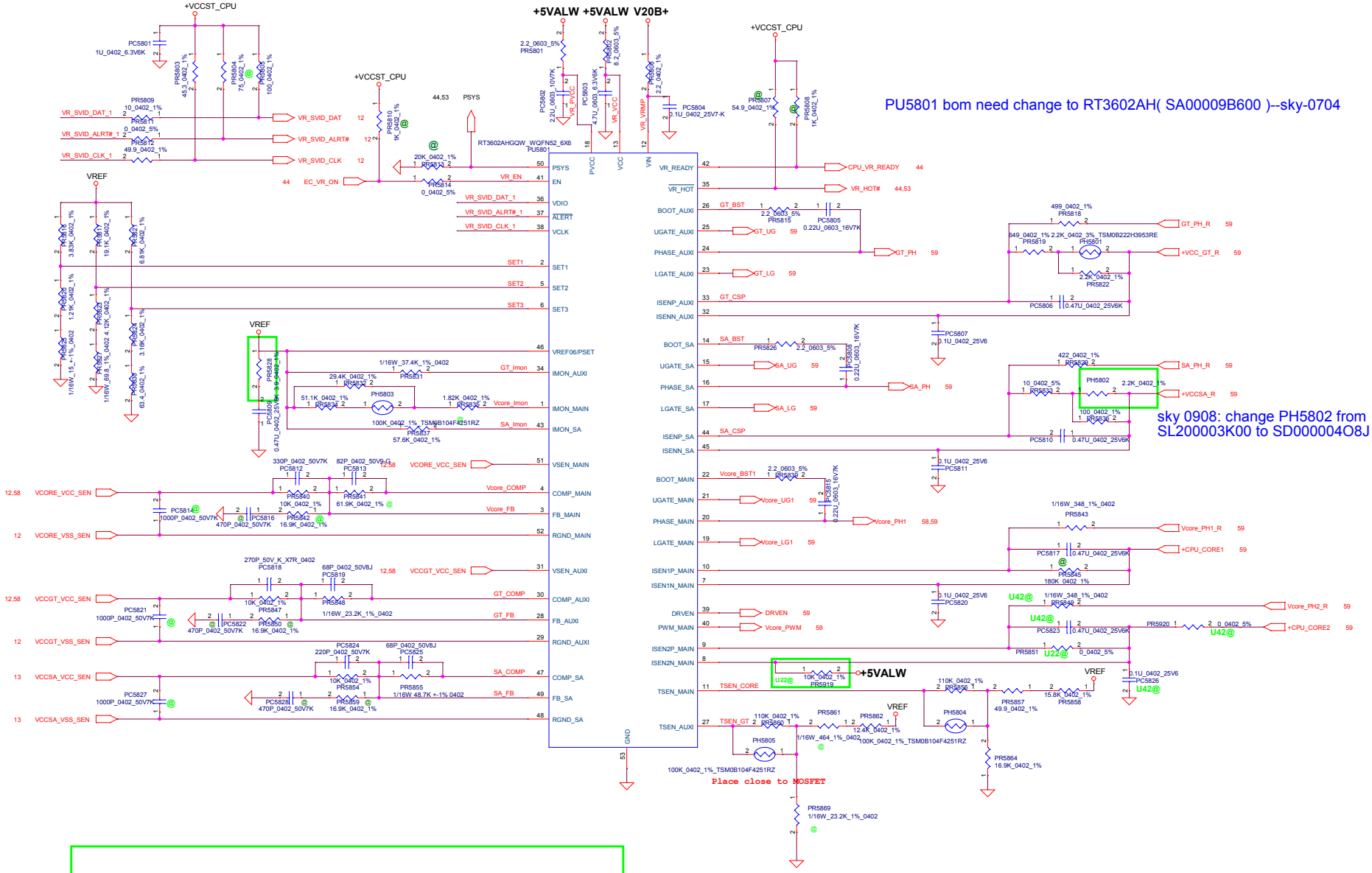

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU-CORE-1

Size: A2 | Document Number: 140S-WHL | Rev: 0.3

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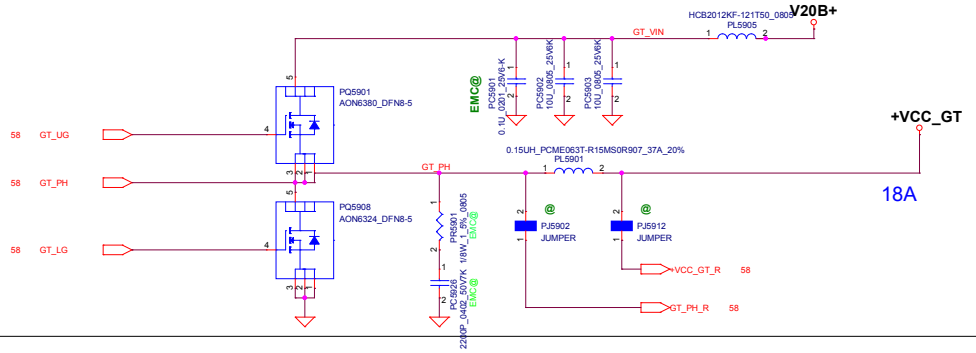
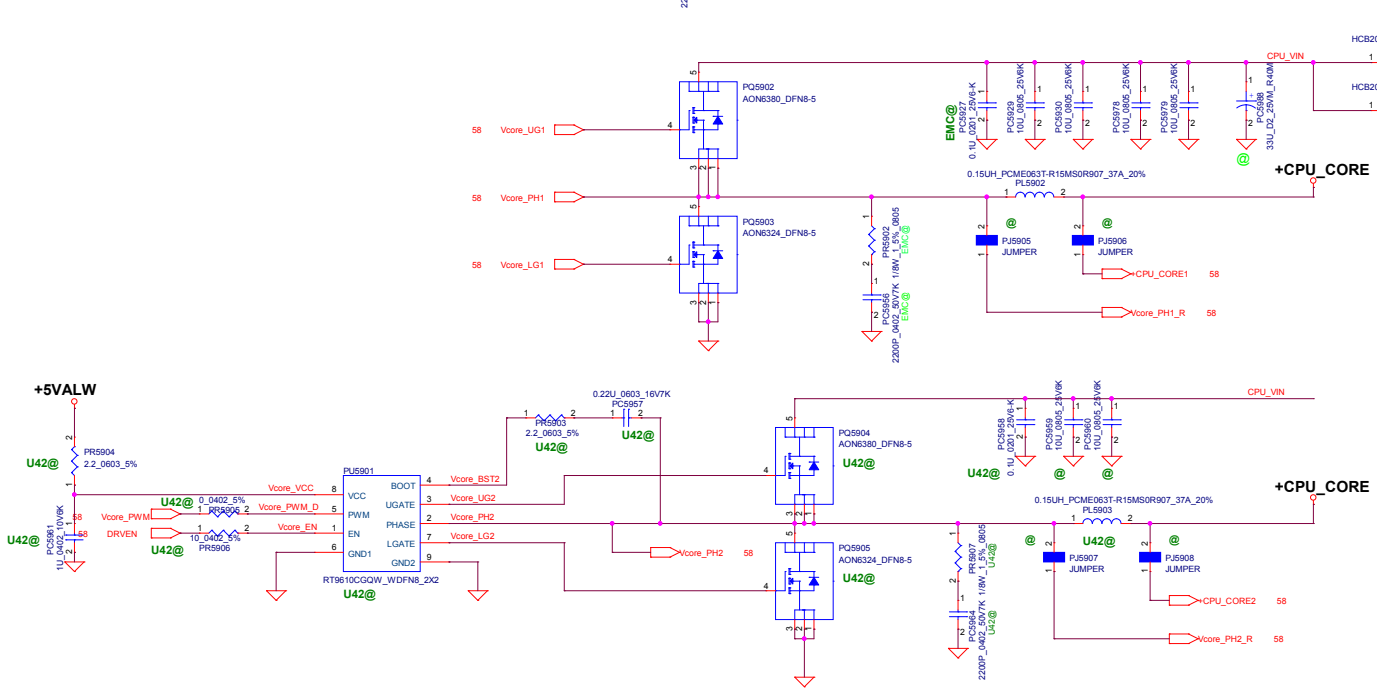


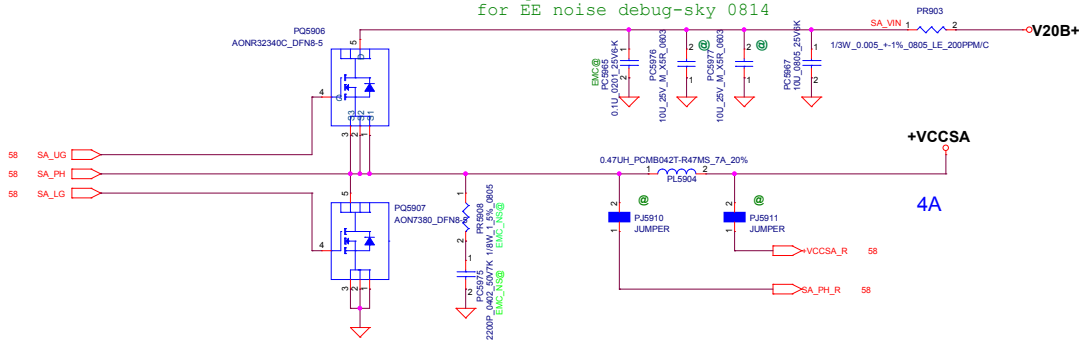
Vboot=0V Loadline=3.1mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=18A Iccmax=31A OCP=37A
OVP=VID+370mV~VID+430mV
Max Overshoot:70mv/10us
UVP=VID-370mV~VID-225mV
Fsw=550Khz



U22 :21A
U42: 48A

Vboot=0V Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=21A/48A Iccmax=32A/70A
OCP=37A / 74A
Max Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz

ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814



Vboot=0V Loadline=10.3Ω
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=4A Iccmax=4.5A OCP=7A
Max Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU-CORE-2

Size: A2 | Document Number: 140S-WHL | Rev: 0.3

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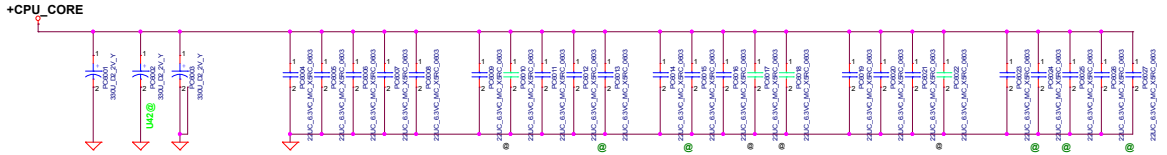
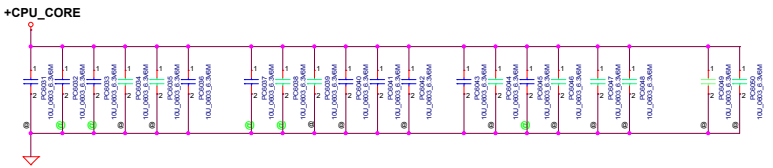


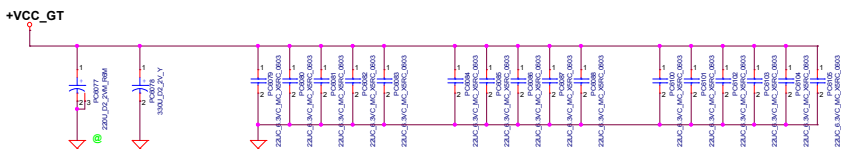
CPU_CORE: 2PCS_330U_D2_2V+1PCS_220U_D2_2V
+13PCS_22U_0603_6V+18PCS_10U_0402_6V
+16PCS_1U_0201_6V=

Vender modify_20180705
PC6003 @ and stuff 6 pcs 22U/0603

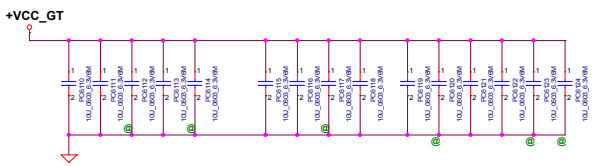
sky modify_20180709
change 10U/0402 to 10U/0603, 1U/0201 to 1U/0402

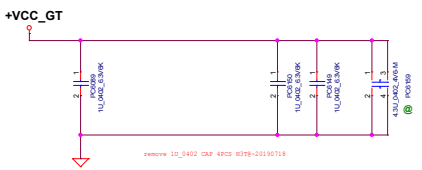
sky modify_20180925
layout change PC6024/PC6025 to PC6036/PC6046



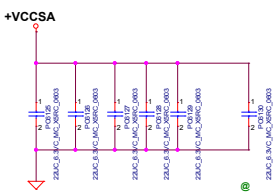


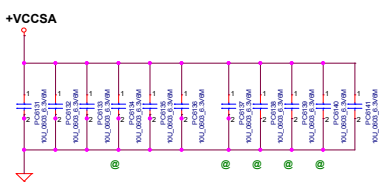
VCCGT: 1PCS_330U_D2_2V+1PCS_220U_D2_2V
+10PCS_22U_0603_6V+9PCS_9U_0603_6V
+2PCS_1U_0402_6V= sky_07_09

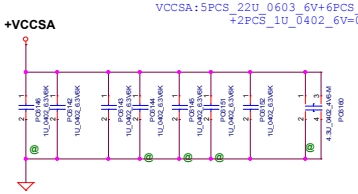




VCCSA:5PCS_22U_0603_6V+6PCS_10U_0603_6V
+2PCS_1U_0402_6V=07-09 sky







Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU Decoupling Cap

Size	Document Number	Rev
Custom	140S-WHL	0.3

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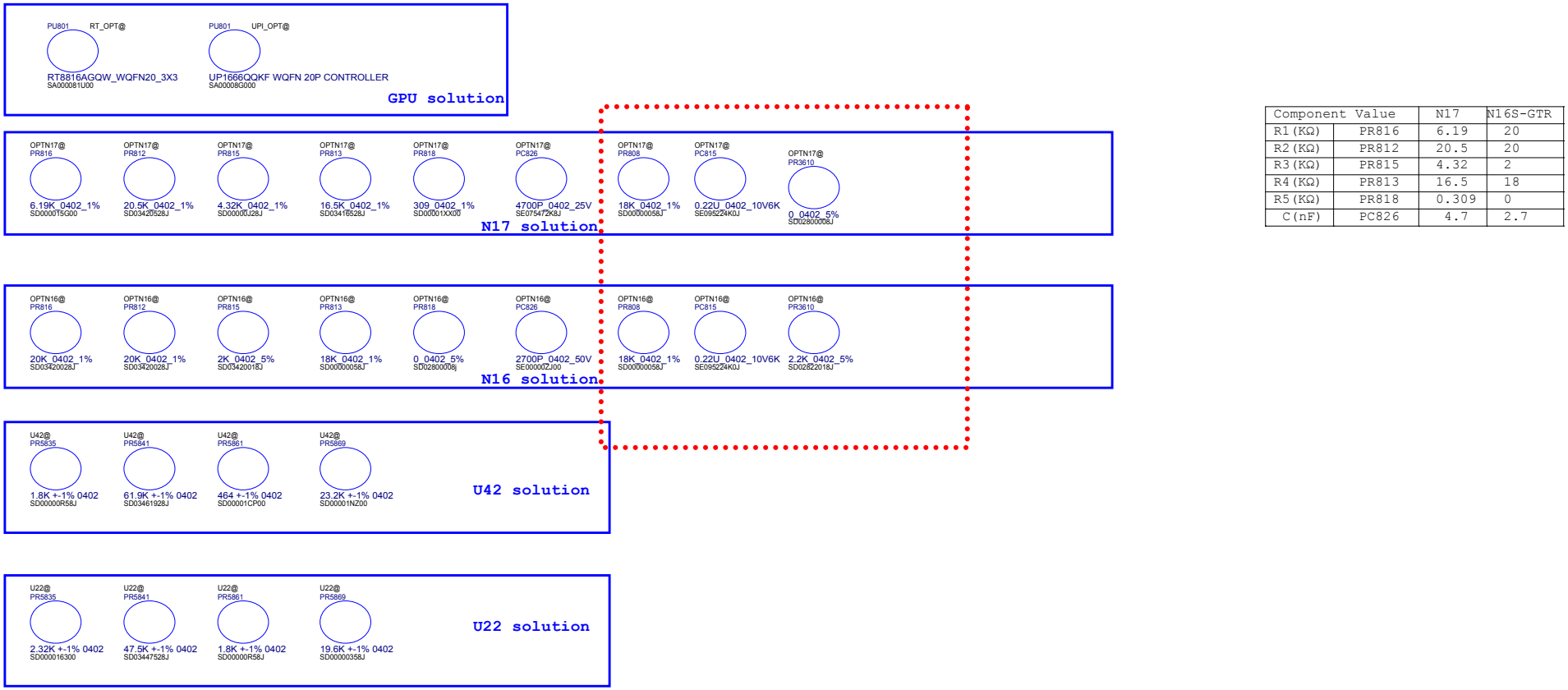

Component Value		N17	N16S-GTR
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: NGFF_SSD_1

Size: C | Document Number: EYG10 | Rev: 0.2

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